PTN36241B

USB 3.0 (SuperSpeed) re-driver

Rev. 1.8 — 12 October 2011 Product data sheet

1. General description

PTN36241B is a USB 3.0 (SuperSpeed) re-driver IC that enhances signal quality by performing receive equalization on the deteriorated input signal followed by transmit de-emphasis maximizing system link performance. With its superior differential signal conditioning and enhancement capability, the device delivers significant flexibility and performance scaling for various systems with different PCB trace and cable channel conditions and still benefit from optimum power consumption.

PTN36241B is a dual-channel device that supports data signaling rate of 5 Gbit/s through each channel. PTN36241B has two channels: one channel is facing the USB host, and another channel is facing the USB peripheral or device. Each channel consists of a high-speed Transmit (Tx) differential lane and a high-speed Receive (Rx) differential lane.

PTN36241B has independent 5-level configuration pins for each channel to select receive equalization, transmit de-emphasis and output swing and these pins can be easily configured by board-strapping (e.g., short, open, resistor). To support applications that require greater level of configurability, PTN36241B delivers intelligent multiplexing of I^2C-bus interface onto 5-level configuration pins. By default, the device is configured with the board-strapped levels of configuration pins. When I^2C-bus reads/writes are performed over these multiplexed pins, the device decodes I^2C transactions and configures its internal functions appropriately.

PTN36241B has built-in advanced power management capability that enables significant power savings under various different USB 3.0 Low power modes (U2/U3). It can detect LFPS signaling and link electrical conditions and can dynamically activate/de-activate internal circuitry and logic. The device performs these actions without host software intervention and conserves power.

PTN36241B supports EasyCom that will go through the compliance testing controlled by the internal state machine. No compliance pin is required.

PTN36241B is powered from 3.3 V supply and is available in HVQFN24 4 mm × 4 mm package with 0.5 mm pitch.

2. Features and benefits

2.1 High-speed channel processing

- Supports USB 3.0 specification (SuperSpeed only)
- Support of 2 channels
- Selectable receive equalization on each channel to recover from Inter Symbol Interference (ISI) and high-frequency losses, with provision to choose from five Equalization gain settings per channel

- Selectable transmit de-emphasis and output swing on each channel delivers pre-compensation suited to channel conditions
- Supports pin and I^2C-bus programmable Input Signal Threshold setting to reliably work under different noise environments accommodating sensitivity needs
- Integrated termination resistors provide impedance matching on both transmit and receive sides
- Programmable termination resistor for receiver side
- Automatic receiver termination indication and detection
- Low active power: 330 mW/100 mA (typical), V_{DD} = 3.3 V
- Power-saving states:
  - 53 mW/16 mA (typical) when in U2/U3 states
  - 20 mW/6 mA (typical) when no connection detected
- Excellent differential and common return loss performance
  - 14 dB differential and 15 dB common-mode return loss for 10 MHz to 1250 MHz
- Flow-through pinout to ease PCB layout and minimize crosstalk effects
- Hot Plug capable
- Supports EasyCom that will go through the compliance testing controlled by the internal state machine
- Power supply: V_{DD} = 3.3 V ± 10 %
- HVQFN24 4 mm × 4 mm package, 0.5 mm pitch; exposed center pad for thermal relief and electrical ground
- ESD: 5 kV HBM, 1250 V CDM
- Operating temperature range 0 °C to 85 °C

2.2 Enhancements

- Intelligent I^2C-bus multiplexing and 5-level logic configuration options (with patent-pending quinary pins) delivering ultimate flexibility
- I^2C-bus interface:
  - Standard-mode (100 kbit/s) or Fast-mode (400 kbit/s)
  - 3.3 V tolerant

3. Applications

- Notebook/netbook/nettop platforms
- Docking stations
- Desktop and AIO platforms
- Active cables
- Server and storage platforms
- USB 3.0 peripherals like consumer/storage devices, printers or USB 3.0 capable hubs/repeaters

4. System context diagrams

Figure 1 illustrates PTN36241B usage.

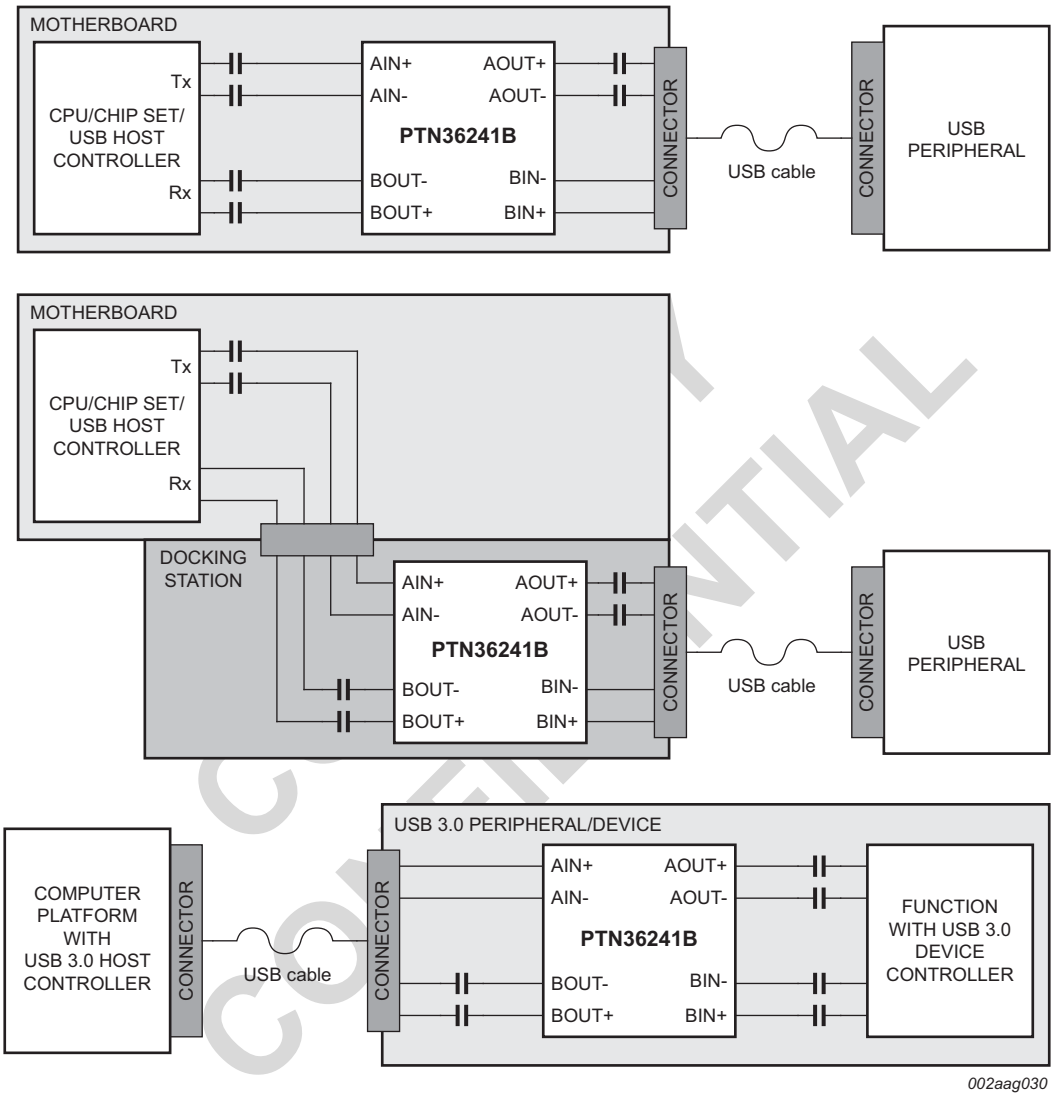


Fig 1. PTN36241B context diagrams

5. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
PTN36241BBS	HVQFN24	plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 4 × 4 × 0.85 mm[1]	SOT616-3

[1] Maximum package height is 1 mm.

6. Block diagram

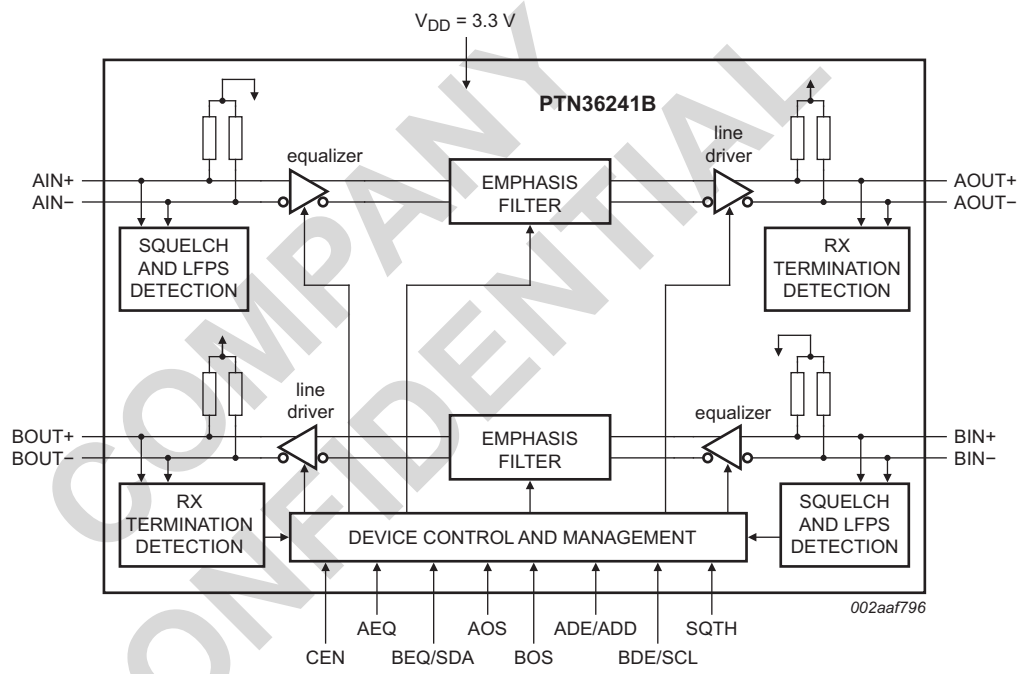


Fig 2. Block diagram of PTN36241B

7. Pinning information

7.1 Pinning

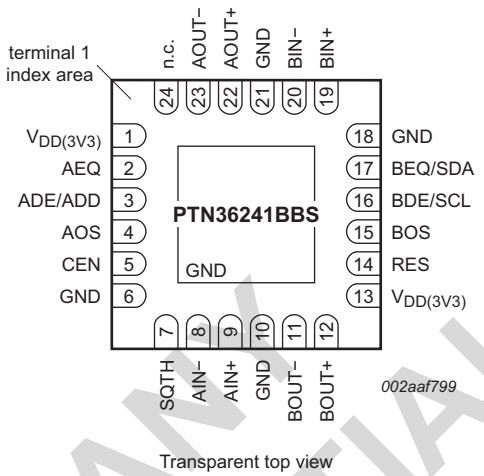


Fig 3. Pin configuration for HVQFN24

7.2 Pin description

Table 2. Pin description

Symbol	Pin	Type	Description
High-speed differential signals			
AIN+	9	self-biasing differential input	Differential signal from USB 3.0 SuperSpeed transmitter. AIN+ makes a differential pair with AIN–. The input to this pin must be AC-coupled externally.
AIN–	8	self-biasing differential input	Differential signal from USB 3.0 SuperSpeed transmitter. AIN– makes a differential pair with AIN+. The input to this pin must be AC-coupled externally.
BOUT+	12	self-biasing differential output	Differential signal to USB 3.0 SuperSpeed receiver. BOUT+ makes a differential pair with BOUT–. The output of this pin must be AC-coupled externally.
BOUT–	11	self-biasing differential output	Differential signal to USB 3.0 SuperSpeed receiver. BOUT– makes a differential pair with BOUT+. The output of this pin must be AC-coupled externally.
AOUT+	22	self-biasing differential output	Differential signal to USB 3.0 SuperSpeed receiver. AOUT+ makes a differential pair with AOUT–. The output of this pin must be AC-coupled externally.

Table 2. Pin description *...continued*

Symbol	Pin	Type	Description
AOUT–	23	self-biasing differential output	Differential signal to USB 3.0 SuperSpeed receiver. AOUT– makes a differential pair with AOUT+. The output of this pin must be AC-coupled externally.
BIN+	19	self-biasing differential input	Differential signal from USB 3.0 SuperSpeed transmitter. BIN+ makes a differential pair with BIN–. The input to this pin must be AC-coupled externally.
BIN–	20	self-biasing differential input	Differential signal from USB 3.0 SuperSpeed transmitter. BIN– makes a differential pair with BIN+. The input to this pin must be AC-coupled externally.
Configuration and control signals			
CEN	5	CMOS input	Chip enable input (active HIGH); internally pulled-up. If CEN is LOW, then the device is in Deep power-saving state even if supply rail is ON; for the device to be able to operate, the CEN pin must be HIGH.
RES	14	CMOS input	Reserved. Tie this pin to ground for normal operation.
AOS	4	input	5-level configuration pin for channel A Tx output swing setting.
BOS	15	input	5-level configuration pin for channel B Tx output swing setting.
AEQ	2	input	5-level configuration pin for channel A Rx equalization gain setting.
BEQ/SDA	17	input/output	5-level configuration pin for channel B Rx equalization gain setting or I^2C-bus data pin.
ADE/ADD	3	input	5-level configuration pin for channel A Tx de-emphasis setting or in I^2C mode, this ADD pin enables selection of 1 out of 4 I^2C-bus device addresses.
BDE/SCL	16	input/output	5-level configuration pin for channel B Tx de-emphasis setting or I^2C-bus clock pin
SQTH	7	input	5-level configuration pin for Channels A and B minimum input signal threshold setting.
n.c.	24	-	not connected
Power supply			
$V_{DD(3V3)}$	1, 13	power	3.3 V supply.
Ground connection			
GND	6, 10, 18, 21	power	Ground.
GND	center pad	power	The center pad must be connected to GND plane for both electrical grounding and thermal relief.

8. Functional description

Refer to Figure 2 “Block diagram of PTN36241B”.

PTN36241B is a USB 3.0 (SuperSpeed) re-driver meant to be used for signal integrity enhancement on various platforms – notebooks, docking, desktop, AIO, peripheral devices etc. With its high fidelity differential signal conditioning capability and wide configurability, this chip is flexible and versatile enough for use under a variety of system environments.

The following sections describe the individual block functions and capabilities of the device in more detail.

8.1 Receive equalization

On the high-speed signal path, the device performs receive equalization providing frequency selective gain based on the configuration pin AEQ (BEQ) setting. Table 3 lists the configuration options available in this device.

Table 3. AEQ (BEQ) configuration options

5-level control input setting AEQ (BEQ)	USB 3.0 (SuperSpeed) signal equalization gain at 2.5 GHz
open	4.5 dB
short to GND	7.5 dB
short to $V_{DD(3V3)}$	9 dB
pull-down resistor to GND[1]	6 dB
pull-up resistor to $V_{DD(3V3)}$[1]	15 dB

[1] The value of these pull-up and pull-down resistors is 75 kΩ.

Please refer also to Section 8.4 for I²C-bus interface based configuration options for Rx equalization of channels A and B.

8.2 Transmit de-emphasis and output swing

The PTN36241B device enhances signal content further by performing de-emphasis on the high-speed signals. In addition, the device can provide flat frequency gain by boosting output signal. Both flat and frequency selective gains prepare the system to cover up for losses further down the link. Table 4 lists de-emphasis and Table 5 lists output swing configuration options of PTN36241B.

Table 4. PTN36241B ADE (BDE) configuration options

5-level control input setting ADE (BDE)	USB 3.0 (SuperSpeed) signal de-emphasis gain
open	–3.5 dB
short to GND	–6.0 dB
short to $V_{DD(3V3)}$	–9.5 dB
pull-down resistor to GND[1]	0 dB
pull-up resistor to $V_{DD(3V3)}$[1]	–6.0 dB

[1] The value of these pull-up and pull-down resistors is 75 kΩ.

Table 5. PTN36241B AOS (BOS) configuration options

5-level control input setting ADE (BDE)	USB 3.0 (SuperSpeed) transmit differential output swing (peak-to-peak)
open	1000 mV
short to GND	850 mV
short to $V_{DD(3V3)}$	1100 mV
pull-down resistor to GND[1]	400 mV
pull-up resistor to $V_{DD(3V3)}$[1]	600 mV

[1] The value of these pull-up and pull-down resistors is 75 kΩ.

Figure 4 illustrates de-emphasis as a function of time for different settings.

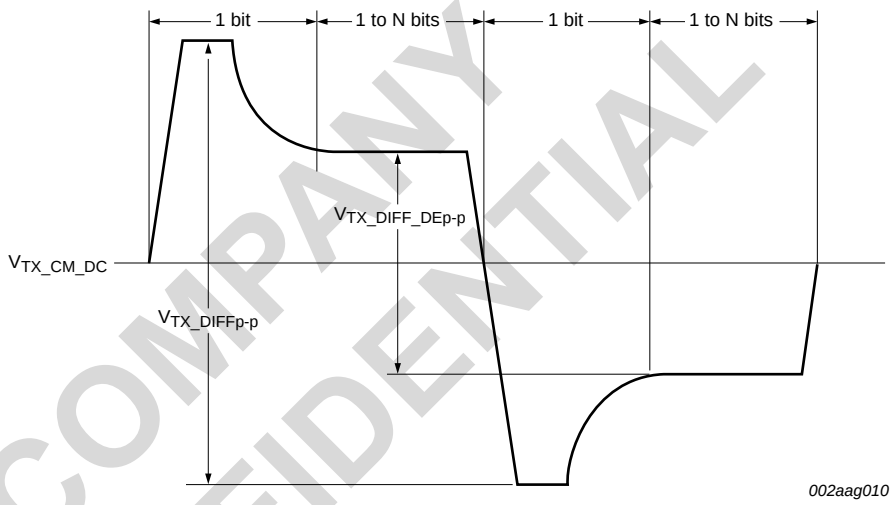


Fig 4. Output with –6 dB de-emphasis

Please refer also to Section 8.4 for I²C-bus interface based configuration options for de-emphasis and output swing of Channels A and B.

8.3 Input signal threshold

To support various platforms that have different noise levels and still maintain sensitivity, PTN36241B provides configuration option to set input signal threshold. When the signal level falls below the threshold, the outputs are squelched and when signal is above the threshold, re-driving function is activated. Table 6 lists the possible input signal threshold configuration options available with this device.

Table 6. SQTH configuration options

5-level control input setting	Channel A input threshold (peak-to-peak)	Channel B input threshold (peak-to-peak)
short to GND	100 mV	100 mV
short to $V_{DD(3V3)}$	125 mV	125 mV
open	75 mV	75 mV
pull-down resistor to GND[1]	150 mV	150 mV
pull-up resistor to $V_{DD(3V3)}$[1]	175 mV	175 mV

[1] The value of these pull-up and pull-down resistors is 75 kΩ.

Please refer also to Section 8.4 for I²C-bus interface based configuration options.

8.4 I²C-bus programmability

PTN36241B has I²C-bus interface that enables system integrator to program register settings suitable for the application needs. Table 7 describes possible settings for different functions of the device. Although the device can be pin configured through board-strapping, it also allows the system integrator to override the settings by programming the internal registers through I²C.

After power-on, the device samples the board-strapped pin values (as I²C is not operational yet) but does not reflect these directly in the register (default) values. So in applications using I²C-bus interface, the system integrator must program the internal registers of the device for proper operation. Further, it is expected that the system integrator performs I²C configuration after power-on and not during normal operation. If such an operation is attempted during normal operation, the device may not behave as specified.

Table 7. I²C-bus registers and description

Values indicated are typical only.

Register offset	Register name	Bit	Reset value	Description
00	A_Tx_Control	7:5	100b	Channel A de-emphasis level. If 0 to 3, set channel A de-emphasis as follows: **0 —** set de-emphasis to 0 dB **1 —** set de-emphasis to –3.5 dB **2 —** set de-emphasis to –6 dB **3 —** set de-emphasis to –9.5 dB If 4 to 7, ADE pin controls channel A de-emphasis level.
		4:0	00000b	Channel A output voltage swing. At Power-On Reset (POR), these bits are set to 0 and AOS quinary pin sets voltage swing. Use these bits to select one of the 24 output levels. If 1 to 24, the channel A output swing is 50 mV times the value of the register. If 0, AOS pin controls channel A Tx output swing level.
01	A_signal_det	7:4	0x8	Controls the channel A squelch level (differential peak-to-peak value). **0000 —** 75 mV **0001 —** 100 mV **0010 —** 125 mV **0011 —** 150 mV **0100 —** 175 mV **0101 —** 200 mV **0110 —** 225 mV **0111 —** 250 mV **1000 to 1111 —** use the value selected by SQTH pin
		3:0	0	Reserved; must be 0.

Table 7. I²C-bus registers and description *…continued*

Values indicated are typical only.

Register offset	Register name	Bit	Reset value	Description
02	A_Rx_termination	7:0	0x8D	Adjusts the A channel receive termination. 0x7C for 40 Ω receive termination 0x8D for 45 Ω receive termination 0xA0 for 50 Ω receive termination
03	A_Equalizer	7:5	0	Reserved; must be 0.
		4:0	0x18	Channel A Rx equalization gain. If 0x18, equalizer setting is controlled by the AEQ quinary pin. **00000b —** 0 dB **00001b —** 1.5 dB **00010b —** 3.0 dB **00011b —** 4.5 dB **00100b —** 6.0 dB **00101b —** 7.5 dB **00110b —** 9.0 dB **00111b —** 10.5 dB **01111b —** 12.0 dB **10111b —** 13.5 dB **11111b —** 15.0 dB **11000b —** AEQ quinary pin sets channel A equalization.
04	B_Tx_control	7:5	100b	Channel B de-emphasis level. If 0 to 3, set channel B de-emphasis as follows: **0 —** set de-emphasis to 0 dB **1 —** set de-emphasis to –3.5 dB **2 —** set de-emphasis to –6 dB **3 —** set de-emphasis to –9.5 dB If 4 to 7, BDE pin controls channel B de-emphasis level.
		4:0	00000b	Channel B output voltage swing. At Power-On Reset (POR), these bits are set to 0 and BOS quinary pin sets voltage swing. Use these bits to select one of the 24 output levels. If 1 to 24, the channel B output swing is 50 mV times the value of the register. If 0, the BOS pin controls channel B Tx output swing level.

Table 7. I²C-bus registers and description *...continued*

Values indicated are typical only.

Register offset	Register name	Bit	Reset value	Description
05	B_signal_det	7:4	0x8	Controls the channel B squelch level (differential peak-to-peak value). **0000 —** 75 mV **0001 —** 100 mV **0010 —** 125 mV **0011 —** 150 mV **0100 —** 175 mV **0101 —** 200 mV **0110 —** 225 mV **0111 —** 250 mV **1000 to 1111 —** use the value selected by SQTH pin
		3:0	0	Reserved; must be 0.
06	B_Rx_termination	7:0	0x8D	Adjusts the B channel receive termination. 0x7C for 40 Ω receive termination 0x8D for 45 Ω receive termination 0xAD for 50 Ω receive termination
07	B_equalizer	7:5	001b	Reserved; must be 001b.
		4:0	0x18	Channel B Rx equalization gain. If 0x18, equlizer setting is controlled by the BEQ quinary pin. **00000b —** 0 dB **00001b —** 1.5 dB **00010b —** 3.0 dB **00011b —** 4.5 dB **00100b —** 6.0 dB **00101b —** 7.5 dB **00110b —** 9.0 dB **00111b —** 10.5 dB **01111b —** 12.0 dB **10111b —** 13.5 dB **11111b —** 15.0 dB **11000b —** BEQ quinary pin sets channel B equalization.
40	I2C_access_enable		0	At POR, this is the only I²C-bus register enabled for reading and writing. Set this register to 0xAE to unlock I²C registers.
44	reset			Writing a 1 to this register will reset the part. This is a self-clearing bit.

8.4.1 I²C-bus read and write operations

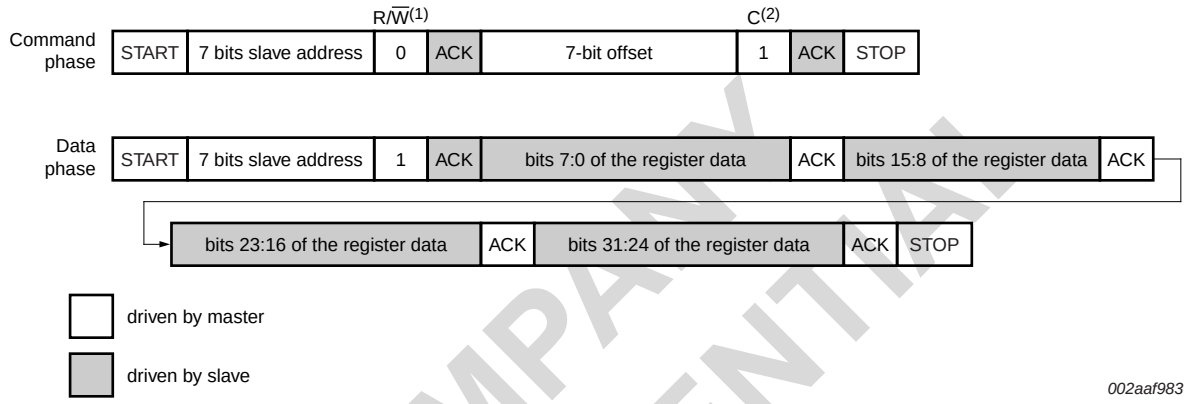
PTN36241B supports programming of the internal registers through the I²C-bus interface. Reading/writing the internal registers must be done according to the following protocol.

The protocol contains two phases:

- Command phase
- Data phase

The command phase is an I²C write to PTN36241B that contains a single data byte. The Least Significant Bit (LSB) indicates if the command that is being executed will read or write data from/to the device. The other 7 bits are the register offset that is used to indicate which register is read or written. The data phase is a second I²C transaction. For a read command, this will be an I²C read operation. For a write command, this will be an I²C write operation.

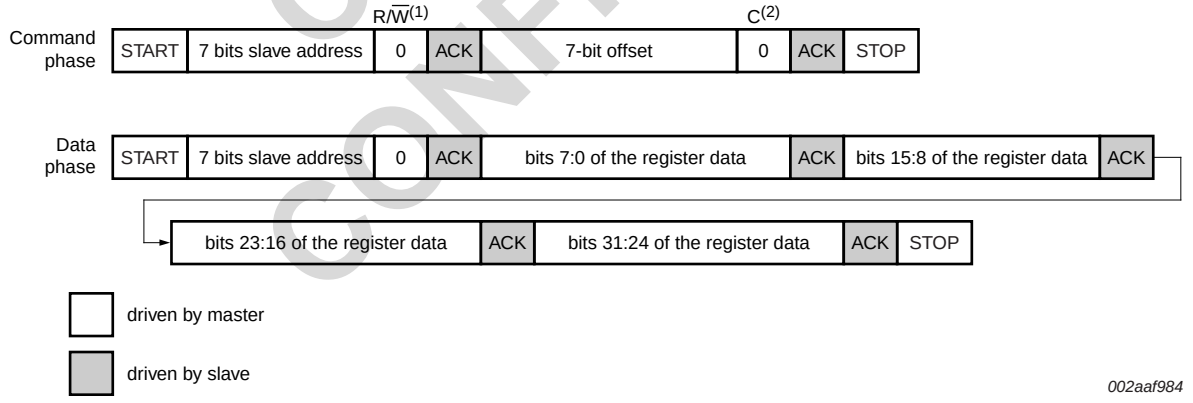
PTN36241B is able to handle both single-byte and 4-byte write/read commands. 4-byte read/write commands are address aligned with 2 LSBs as '0'. Figure 5 illustrates the protocol used on the I²C-bus to read and write registers inside the device.



(1) R/$\overline{W}$ = read/write bit. 0b = I²C write; 1b = I²C read.

(2) C = command bit. 0b = write command; 1b = read command.

a. Read sequence



(1) R/$\overline{W}$ = read/write bit. 0b = I²C write; 1b = I²C read.

(2) C = command bit. 0b = write command; 1b = read command.

b. Write sequence

Fig 5. I²C-bus read and write sequences

Table 8 shows how the PTN36241B device addresses can be selected by using ADD (I^2C-bus device address) pin.

Table 8. Device address selection

ADD pin	7-bit I^2C-bus device address
short to GND	0010010
short to $V_{DD(3V3)}$	0010110
pull-down resistor to GND[1]	0011010
pull-up resistor to $V_{DD(3V3)}$[1]	0011110

[1] The value of these pull-up and pull-down resistors is 75 kΩ.

PTN36241B has built-in I^2C access lock mechanism that helps avoid inadvertent writes/reads into the device. After power-up, only register offset 0x40 can be written by the host controller. So before accessing any register (register offset 0x00 to 0x7, 0x41), the host controller is expected wo write 0xAE at address 0x40. This would open the I^2C lock enabling the host controller to configure the device registers suitably as required for the application.

8.5 Device control — mode, enable, power-on initialization

PTN36241B has a built-in reset circuitry that generates reset signal after power-on. All the internal registers and state machines are initialized and the registers take default values as defined in Table 7.

The CEN enable pin can be toggled asynchronously any time after power-on and the device can be put in Active or Deep power-saving state.

- When CEN is HIGH, the device is in Active state and when it is LOW, device is in Deep power-saving state.
- The values of the configuration pins (AEQ, ADE, BEQ, BDE, AOS, BOS, SQTH) are sampled on power-on and whenever CEN is toggled asynchronously any time afterwards.
- When CEN is toggled LOW to HIGH, the device will undergo an equivalent of power-on reset operation. All registers/state machines will be put to power-on condition.

The normal functioning of the re-driver is not guaranteed when the configuration and/or control pins are being changed. The typical device usage is to set these control and configuration pins to pre-determined levels at power-on and not to change thereafter.

8.6 Device states and power management

PTN36241B has implemented an advanced power management scheme that operates in tune with USB 3.0 bus electrical condition. Although the device does not decode USB power management commands (related to USB 3.0 U1/U2/U3 transitions) exchanged between USB 3.0 host and peripheral/device, it relies on bus electrical conditions and control pins/register settings to decide to be in one of the following states:

- **Active state** wherein device is fully operational, USB data is transported on channels A and B. In this state, USB connection exists and the Receive Termination indication remains active. But there is no need for Receive Termination detection.
- **Power-saving** state wherein the channels A and B are kept enabled. In this state, squelching, LFPS detection and/or Receive termination detection circuitry are active. Based on USB connection, there are 2 possibilities:
  - No USB connection:

    Receive Termination detection circuitry keeps polling periodically.

    Receive Termination indication is not active.
  - When USB connection exists and when the link is in USB 3.0 U2/U3 mode:

    Receive Termination detection circuitry keeps polling periodically.

    Receive Termination indication is active.
- **Deep power-saving** or **Shutdown state** wherein the channel is in Deep power-saving/Shutdown condition enabling significant power saving.
  - DC common-mode voltage level is not maintained.
  - Tx and Rx terminations are put to high-impedance condition.
  - Transitioning to Active state would take several tens of microseconds.

Receive termination detection circuitry is implemented as part of a transmitter and detect whether a load device with equivalent DC impedance Z_{RX_DC} is present.

9. Limiting values

Table 9. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DD(3V3)}$	supply voltage (3.3 V)		[1]	–0.3	+4.6	V
V_I	input voltage		[1]	–0.3	$V_{DD(3V3)}$ + 0.5	V
T_{stg}	storage temperature			–65	+150	°C
V_{ESD}	electrostatic discharge voltage	HBM	[2]	-	5000	V
		CDM	[3]	-	1250	V

[1] All voltage values (except differential voltages) are with respect to network ground terminal.

[2] Human Body Model: ANSI/EOS/ESD-S5.1-1994, standard for ESD sensitivity testing, Human Body Model - Component level; Electrostatic Discharge Association, Rome, NY, USA.

[3] Charged Device Model; ANSI/EOS/ESD-S5.3-1-1999, standard for ESD sensitivity testing, Charged Device Model - Component level; Electrostatic Discharge Association, Rome, NY, USA.

10. Recommended operating conditions

Table 10. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	supply voltage	3.3 V supply option	3.0	3.3	3.6	V
V_I	input voltage	open-drain I/O with respect to ground (e.g., SCL, SDA)	-	$V_{DD(3V3)}$	-	V
		control and configuration pins (e.g., AEQ, BEQ, ADE, BDE, AOS, BOS, SQTH)	-	$V_{DD(3V3)}$	-	V
T_{amb}	ambient temperature	operating in free air	0	-	85	°C

11. Characteristics

11.1 Device characteristics

Table 11. Device characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{startup}$	start-up time	supply voltage within operating range to specified operating characteristics	-	-	20	ms
$t_{s(LH)}$	LOW to HIGH settling time	disable to enable; CEN LOW → HIGH change to specified operating characteristics; device is supplied with valid supply voltage	-	-	1	ms
$t_{s(HL)}$	HIGH to LOW settling time	enable to disable; CEN HIGH → LOW change to specified operating characteristics; device is supplied with valid supply voltage	-	-	1	ms
t_{rcfg}	reconfiguration time	any quinary configuration pin change (AEQ, BEQ, ADE, BDE, AOS, BOS, SQTH - from one setting to another setting) to specified operating characteristics; device is supplied with valid supply voltage; reconfiguration can be triggered by CEN toggle	-	-	100	µs
$t_{PD(dif)}$	differential propagation delay	between 50 % level at input and output; see Figure 6	-	-	1	ns
t_{idle}	idle time	default wait time to wait before getting into U2/U3 Power-saving states	-	300	-	ms
t_{ps_exit}	power-saving state exit time	time for exiting from Power-saving state and get into Active state; see Figure 8	-	10	-	µs
t_{idle_entry}	idle entry time	reaction time for squelch detection circuit; see Figure 7	-	-	54	ns
t_{idle_exit}	idle exit time	reaction time for squelch detection circuit; see Figure 7	-	4	6	ns
I_{DD}	supply current	Active state; Rx equalization = 15 dB; Tx output signal swing = 400 mV (differential peak-to-peak value); Tx de-emphasis = 0 dB	-	100	-	mA
		U2/U3 Power-saving state	-	16	-	mA
		no USB connection state	-	6	-	mA
		Deep power-saving state; CEN = LOW	-	-	3.5	mA

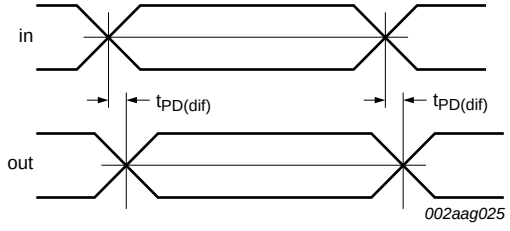


Fig 6. Propagation delay

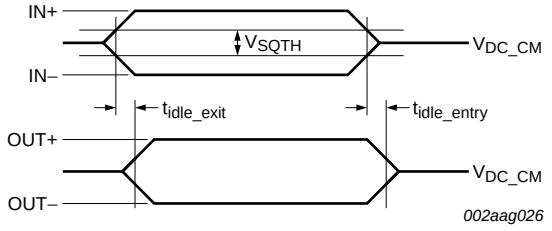


Fig 7. Electrical idle transitions in U0/U1 modes

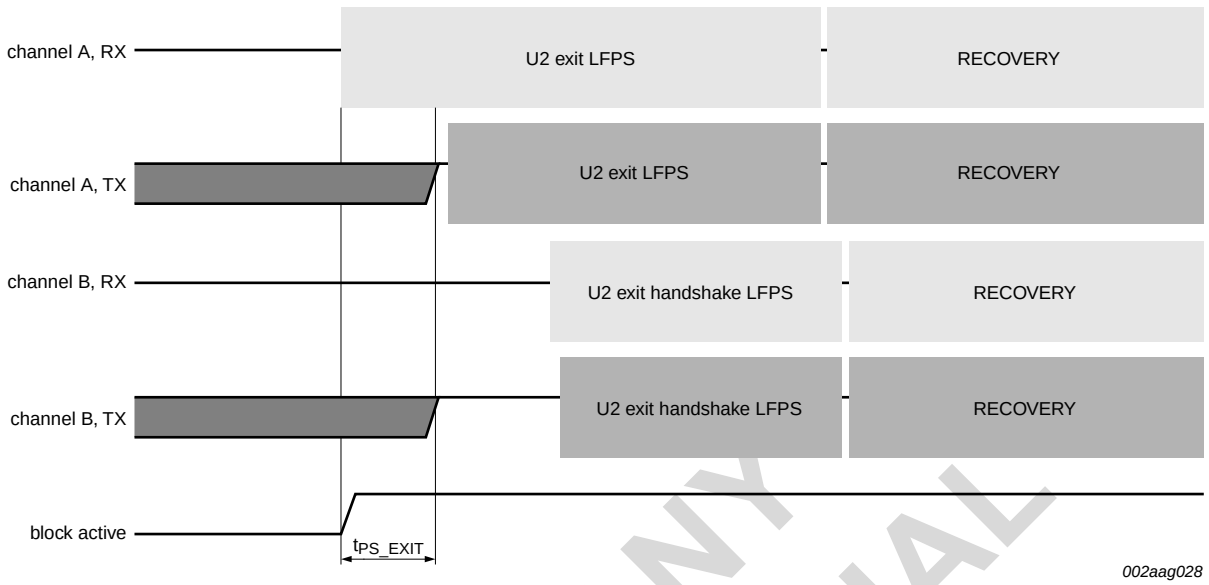


Fig 8. U2/U3 exit behavior

11.2 Receiver AC/DC characteristics

Table 12. Receiver AC/DC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Z_{RX_DC}	DC input impedance	common-mode	20	-	28	Ω
ΔZ_i	differential input impedance	RX pair	72	-	120	Ω
Z_{IH}	HIGH-level input impedance	DC input	25	-	-	kΩ
$V_{RX\_DIFFp-p}$	differential input peak-to-peak voltage		75	-	1200	mV
$V_{RX\_DC\_CM}$	RX DC common mode voltage		-	1.8	-	V
$V_{RX\_AC\_CM}$	RX AC common-mode voltage	peak	-	-	150	mV
$V_{th(i)}$	input threshold voltage	differential peak-to-peak value	75	-	300	mV

11.3 Transmitter AC/DC characteristics

Table 13. Transmitter AC/DC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Z_{TX_DC}	transmitter DC impedance	common-mode	18	-	30	Ω
$Z_{TX\_DIFF\_DC}$	TX differential impedance		72	-	120	Ω
$V_{TX\_DIFFp-p}$	differential peak-to-peak output voltage	typical level decided by configuration pin/I^2C register setting	400	-	1200	mV
$V_{TX\_DC\_CM}$	TX DC common-mode output voltage		1.2	-	1.65	V
$V_{TX\_CM\_ACpp\_ACTIVE}$	TX AC common-mode output voltage in active state (peak-to-peak)	device input fed with differential signal	-	-	100	mV
$V_{TX\_IDLE\_DIFF\_ACpp}$	TX AC differential output voltage (peak-to-peak)	when link is in electrical idle	-	-	10	mV
V_{DETECT}	voltage change allowed during receiver detection	positive voltage swing to sense the receiver termination detection	-	-	600	mV
$t_{r(TX)}$	TX rise time	measured using 20 % and 80 % levels; see Figure 9	30	50	-	ps
$t_{f(TX)}$	TX fall time	measured using 80 % and 20 % levels; see Figure 9	30	50	-	ps
$t_{TX\_RF\_MIS}$	TX rise/fall time mismatch	measured using 20 % and 80 % levels	-	-	20	ps

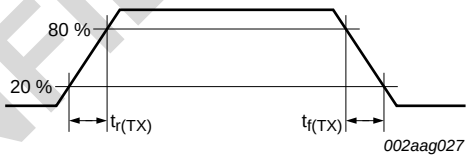


Fig 9. Output rise and fall times

11.4 Jitter performance

Table 14 provides jitter performance of PTN36241B under a specific set of conditions that is illustrated by Figure 6.

Table 14. Jitter performance characteristics

Unit Interval (UI) = 200 ps.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{jit(o)(p-p)}$	peak-to-peak output jitter time	total jitter at test point C	[1]	-	0.19	-	UI
$t_{DJ(p-p)}$	peak-to-peak deterministic jitter time		[1]	-	0.11	-	UI
$t_{RJ(p-p)}$	peak-to-peak random jitter time		[1][2]	-	0.08	-	UI

[1] Measured at test point C with K28.5 pattern, V_{ID} = 1000 mV (peak-to-peak), 5 Gbit/s; –3.5 dB de-emphasis from source.

[2] Random jitter calculated as 14.069 times the RMS random jitter for 10^{-12} bit error rate.

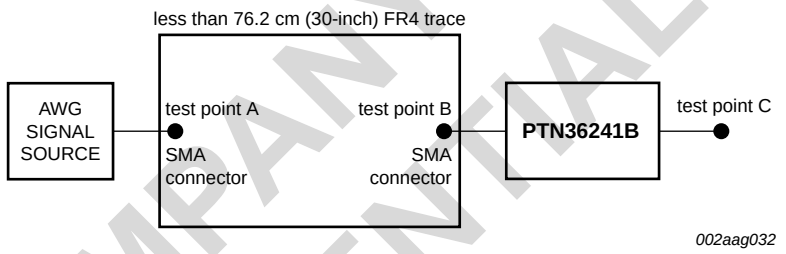


Fig 10. Jitter measurement setup

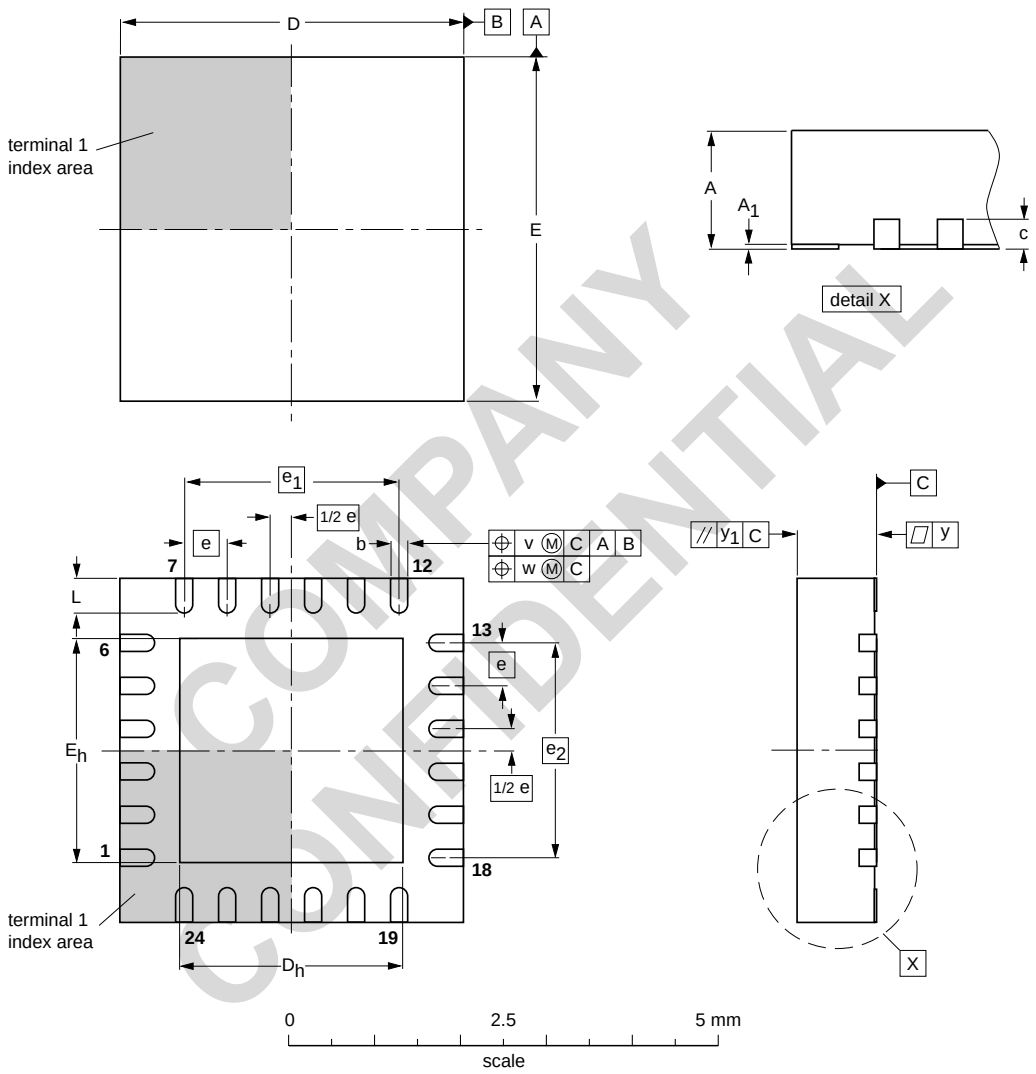
11.5 Control inputs

Table 15. CMOS control input characteristics (CEN and RES pins)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage		$0.65 \times V_{DD(3V3)}$	-	-	V
V_{IL}	LOW-level input voltage		-	-	$0.35 \times V_{DD(3V3)}$	V
I_{LI}	input leakage current	measured with input at $V_{IH(max)}$ and $V_{IL(min)}$	-	-	25	µA

12. Package outline

HVQFN24: plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 4 x 4 x 0.85 mm **SOT616-3**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	4.1 3.9	2.75 2.45	4.1 3.9	2.75 2.45	0.5	2.5	2.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT616-3	- - -	MO-220	- - -			~~04-11-19~~ 05-03-10

Fig 11. Package outline SOT616-3 (HVQFN24)

13. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

13.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

13.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

13.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

13.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 12) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 16 and 17

Table 16. SnPb eutectic process (from J-STD-020C)

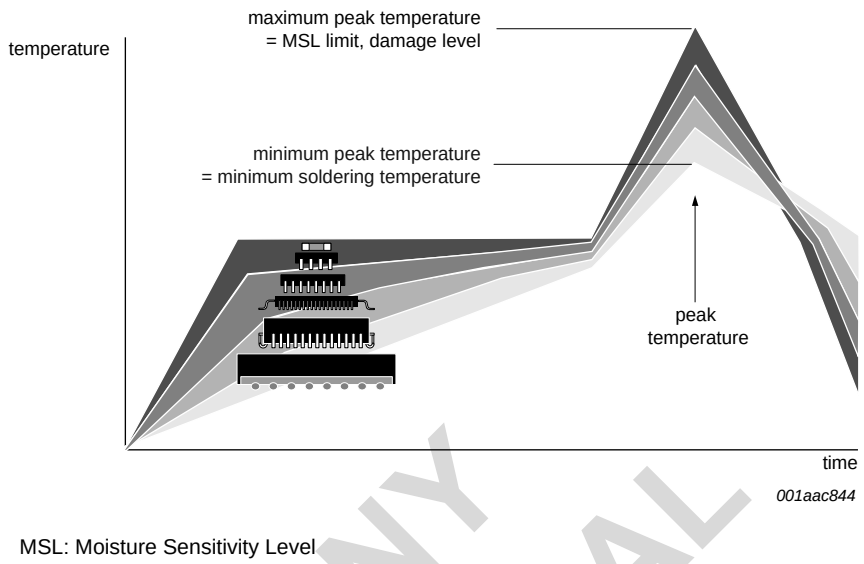
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 17. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 12.



MSL: Moisture Sensitivity Level

Fig 12. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

14. Abbreviations

Table 18. Abbreviations

Acronym	Description
AIO	All In One
CDM	Charged-Device Model
ESD	ElectroStatic Discharge
HBM	Human Body Model
I^2C-bus	Inter-Integrated Circuit bus
I/O	Input/Output
IC	Integrated Circuit
ISI	Inter Symbol Interference
LFPS	Low Frequency Periodic Signaling
PCB	Printed-Circuit Board
SI	Signal Integrity
USB	Universal Serial Bus

15. Revision history

Table 19. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PTN36241B v.1.8	20111012	Product data sheet	-	PTN36241B v.1.7
PTN36241B v.1.7	20111006	Product data sheet	-	PTN36241B v.1.6
PTN36241B v.1.6	20110830	Preliminary data sheet	-	PTN36241B v.1.5
PTN36241B v.1.5	20110610	Preliminary data sheet	-	PTN36241B v.1.4
PTN36241B v.1.4	20110602	Objective data sheet	-	PTN36241B v.1.3
PTN36241B v.1.3	20110210	Objective data sheet	-	PTN36241B v.1.2
PTN36241B v.1.2	20110201	Objective data sheet	-	PTN36241A_241B v.1.1
PTN36241A_241B v.1.1	20101028	Objective data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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