



## K10 Sub-Family Data Sheet

Supports the following:

MK10DN32VLF5, MK10DX32VLF5,  
MK10DN64VLF5, MK10DX64VLF5,  
MK10DN128VLF5, MK10DX128VLF5,  
MK10DN32VFT5, MK10DX32VFT5,  
MK10DN64VFT5, MK10DX64VFT5,  
MK10DN128VFT5, MK10DX128VFT5

### Features

- Operating Characteristics
  - Voltage range: 1.71 to 3.6 V
  - Flash write voltage range: 1.71 to 3.6 V
  - Temperature range (ambient): -40 to 105°C
- Performance
  - Up to 50 MHz ARM Cortex-M4 core with DSP instructions delivering 1.25 Dhystone MIPS per MHz
- Memories and memory interfaces
  - Up to 128 KB program flash.
  - Up to 32 KB FlexNVM on FlexMemory devices
  - 2 KB FlexRAM on FlexMemory devices
  - Up to 16 KB RAM
  - Serial programming interface (EzPort)
- Clocks
  - 3 to 32 MHz crystal oscillator
  - 32 kHz crystal oscillator
  - Multi-purpose clock generator
- System peripherals
  - Multiple low-power modes to provide power optimization based on application requirements
  - 4-channel DMA controller, supporting up to 41 request sources
  - External watchdog monitor
  - Software watchdog
  - Low-leakage wakeup unit
- Security and integrity modules
  - Hardware CRC module to support fast cyclic redundancy checks
  - 128-bit unique identification (ID) number per chip

## K10P48M50SF0



- Human-machine interface
  - Low-power hardware touch sensor interface (TSI)
  - General-purpose input/output
- Analog modules
  - 16-bit SAR ADC
  - Two analog comparators (CMP) containing a 6-bit DAC and programmable reference input
  - Voltage reference
- Timers
  - Programmable delay block
  - Eight-channel motor control/general purpose/PWM timer
  - Two-channel quadrature decoder/general purpose timer
  - Periodic interrupt timers
  - 16-bit low-power timer
  - Carrier modulator transmitter
  - Real-time clock
- Communication interfaces
  - USB full-/low-speed On-the-Go controller with on-chip transceiver
  - SPI module
  - I2C module
  - Three UART modules
  - I2S module

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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# 1 Ordering parts

## 1.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to <http://www.freescale.com> and perform a part number search for the following device numbers: PK10 and MK10.

# 2 Part identification

## 2.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

## 2.2 Format

Part numbers for this device have the following format:

Q K## A M FFF R T PP CC N

## 2.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	<ul style="list-style-type: none"> <li>M = Fully qualified, general market flow</li> <li>P = Prequalification</li> </ul>
K##	Kinetis family	<ul style="list-style-type: none"> <li>K10</li> </ul>
A	Key attribute	<ul style="list-style-type: none"> <li>D = Cortex-M4 w/ DSP</li> <li>F = Cortex-M4 w/ DSP and FPU</li> </ul>
M	Flash memory type	<ul style="list-style-type: none"> <li>N = Program flash only</li> <li>X = Program flash and FlexMemory</li> </ul>

*Table continues on the next page...*

## Terminology and guidelines

Field	Description	Values
FFF	Program flash memory size	<ul style="list-style-type: none"> <li>• 32 = 32 KB</li> <li>• 64 = 64 KB</li> <li>• 128 = 128 KB</li> <li>• 256 = 256 KB</li> <li>• 512 = 512 KB</li> <li>• 1M0 = 1 MB</li> </ul>
R	Silicon revision	<ul style="list-style-type: none"> <li>• Z = Initial</li> <li>• (Blank) = Main</li> <li>• A = Revision after main</li> </ul>
T	Temperature range (°C)	<ul style="list-style-type: none"> <li>• V = -40 to 105</li> <li>• C = -40 to 85</li> </ul>
PP	Package identifier	<ul style="list-style-type: none"> <li>• FM = 32 QFN (5 mm x 5 mm)</li> <li>• FT = 48 QFN (7 mm x 7 mm)</li> <li>• LF = 48 LQFP (7 mm x 7 mm)</li> <li>• LH = 64 LQFP (10 mm x 10 mm)</li> <li>• MP = 64 MAPBGA (5 mm x 5 mm)</li> <li>• LK = 80 LQFP (12 mm x 12 mm)</li> <li>• MB = 81 MAPBGA (8 mm x 8 mm)</li> <li>• LL = 100 LQFP (14 mm x 14 mm)</li> <li>• ML = 104 MAPBGA (8 mm x 8 mm)</li> <li>• MC = 121 MAPBGA (8 mm x 8 mm)</li> <li>• LQ = 144 LQFP (20 mm x 20 mm)</li> <li>• MD = 144 MAPBGA (13 mm x 13 mm)</li> <li>• MF = 196 MAPBGA (15 mm x 15 mm)</li> <li>• MJ = 256 MAPBGA (17 mm x 17 mm)</li> </ul>
CC	Maximum CPU frequency (MHz)	<ul style="list-style-type: none"> <li>• 5 = 50 MHz</li> <li>• 7 = 72 MHz</li> <li>• 10 = 100 MHz</li> <li>• 12 = 120 MHz</li> <li>• 15 = 150 MHz</li> </ul>
N	Packaging type	<ul style="list-style-type: none"> <li>• R = Tape and reel</li> <li>• (Blank) = Trays</li> </ul>

## 2.4 Example

This is an example part number:

MK10DN32VLF5

## 3 Terminology and guidelines

## 3.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

### 3.1.1 Example

This is an example of an operating requirement, which you must meet for the accompanying operating behaviors to be guaranteed:

Symbol	Description	Min.	Max.	Unit
$V_{DD}$	1.0 V core supply voltage	0.9	1.1	V

## 3.2 Definition: Operating behavior

An *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

### 3.2.1 Example

This is an example of an operating behavior, which is guaranteed if you meet the accompanying operating requirements:

Symbol	Description	Min.	Max.	Unit
$I_{WP}$	Digital I/O weak pullup/ pulldown current	10	130	$\mu A$

## 3.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

### 3.3.1 Example

This is an example of an attribute:

Symbol	Description	Min.	Max.	Unit
CIN_D	Input capacitance: digital pins	—	7	pF

## 3.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

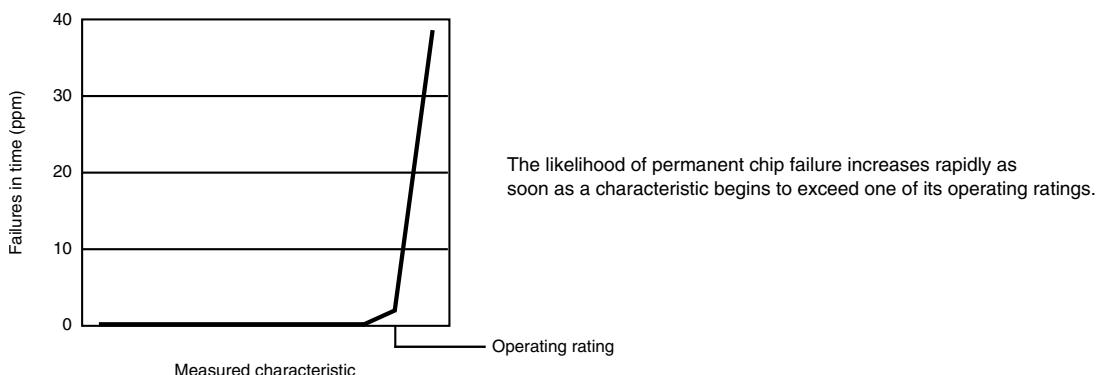
- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

### 3.4.1 Example

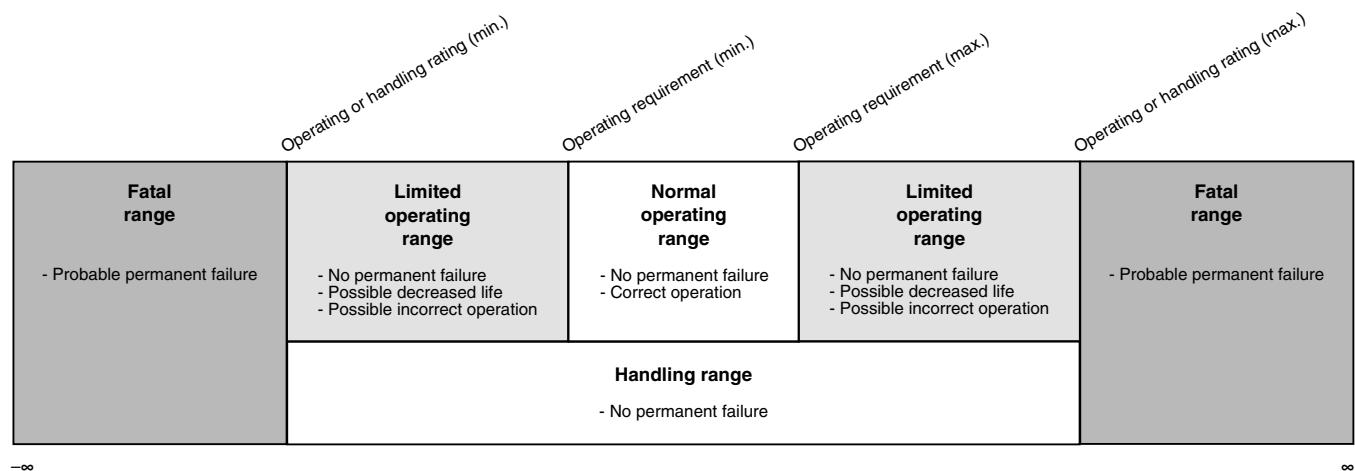
This is an example of an operating rating:

Symbol	Description	Min.	Max.	Unit
V <sub>DD</sub>	1.0 V core supply voltage	-0.3	1.2	V

## 3.5 Result of exceeding a rating



### **3.6 Relationship between ratings and operating requirements**



### **3.7 Guidelines for ratings and operating requirements**

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
  - During normal operation, don't exceed any of the chip's operating requirements.
  - If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

### 3.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
  - Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

### 3.8.1 Example 1

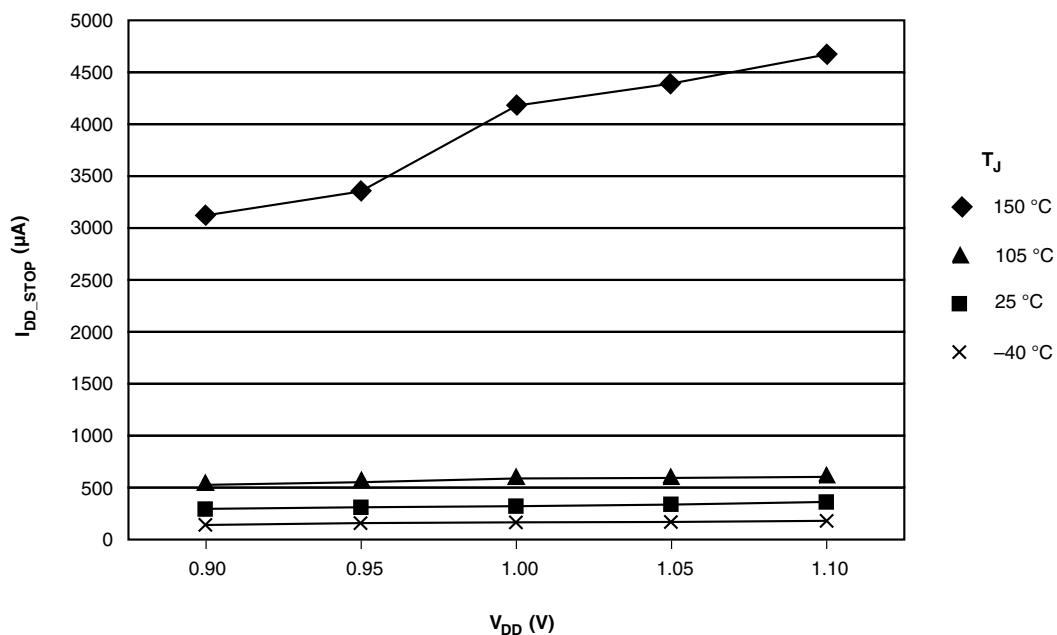
This is an example of an operating behavior that includes a typical value:

## Ratings

Symbol	Description	Min.	Typ.	Max.	Unit
I <sub>WP</sub>	Digital I/O weak pullup/pulldown current	10	70	130	µA

### 3.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:



## 3.9 Typical value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Symbol	Description	Value	Unit
T <sub>A</sub>	Ambient temperature	25	°C
V <sub>DD</sub>	3.3 V supply voltage	3.3	V

## 4 Ratings

## 4.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T <sub>STG</sub>	Storage temperature	-55	150	°C	<a href="#">1</a>
T <sub>SDR</sub>	Solder temperature, lead-free	—	260	°C	<a href="#">2</a>

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

## 4.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	<a href="#">1</a>

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

## 4.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V <sub>HBM</sub>	Electrostatic discharge voltage, human body model	-2000	+2000	V	<a href="#">1</a>
V <sub>CDM</sub>	Electrostatic discharge voltage, charged-device model	-500	+500	V	<a href="#">2</a>
I <sub>LAT</sub>	Latch-up current at ambient temperature of 105°C	-100	+100	mA	

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.

## 4.4 Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit
V <sub>DD</sub>	Digital supply voltage	-0.3	3.8	V
I <sub>DD</sub>	Digital supply current	—	155	mA
V <sub>DIO</sub>	Digital input voltage (except RESET, EXTAL, and XTAL)	-0.3	V <sub>DD</sub> + 0.3	V
V <sub>AIO</sub>	Analog <sup>1</sup> , RESET, EXTAL, and XTAL input voltage	-0.3	V <sub>DD</sub> + 0.3	V

Table continues on the next page...

## General

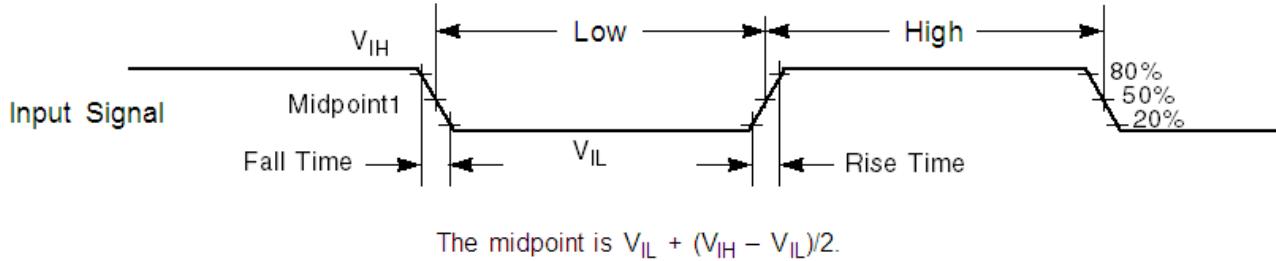
Symbol	Description	Min.	Max.	Unit
$I_D$	Instantaneous maximum current single pin limit (applies to all port pins)	-25	25	mA
$V_{DDA}$	Analog supply voltage	$V_{DD} - 0.3$	$V_{DD} + 0.3$	V
$V_{USB\_DP}$	USB_DP input voltage	-0.3	3.63	V
$V_{USB\_DM}$	USB_DM input voltage	-0.3	3.63	V
$V_{REGIN}$	USB regulator input	-0.3	6.0	V
$V_{BAT}$	RTC battery supply voltage	-0.3	3.8	V

1. Analog pins are defined as pins that do not have an associated general purpose I/O port function.

## 5 General

### 5.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.



The midpoint is  $V_{IL} + (V_{IH} - V_{IL})/2$ .

**Figure 1. Input signal measurement reference**

All digital I/O switching characteristics assume:

1. output pins
  - have  $C_L=30\text{pF}$  loads,
  - are configured for fast slew rate ( $\text{PORTx\_PCRn[SRE]}=0$ ), and
  - are configured for high drive strength ( $\text{PORTx\_PCRn[DSE]}=1$ )
2. input pins
  - have their passive filter disabled ( $\text{PORTx\_PCRn[PFE]}=0$ )

### 5.2 Nonswitching electrical specifications

## 5.2.1 Voltage and current operating requirements

Table 1. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
$V_{DD}$	Supply voltage	1.71	3.6	V	
$V_{DDA}$	Analog supply voltage	1.71	3.6	V	
$V_{DD} - V_{DDA}$	$V_{DD}$ -to- $V_{DDA}$ differential voltage	-0.1	0.1	V	
$V_{SS} - V_{SSA}$	$V_{SS}$ -to- $V_{SSA}$ differential voltage	-0.1	0.1	V	
$V_{BAT}$	RTC battery supply voltage	1.71	3.6	V	
$V_{IH}$	Input high voltage	$0.7 \times V_{DD}$ $0.75 \times V_{DD}$	— —	V V	1
$V_{IL}$	Input low voltage				
	• $2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	$0.35 \times V_{DD}$ $0.3 \times V_{DD}$	— —	V V	1
	• $1.7 \text{ V} \leq V_{DD} \leq 2.7 \text{ V}$				
$V_{HYS}$	Input hysteresis	$0.06 \times V_{DD}$	—	V	
$I_{ICIO}$	I/O pin DC injection current — single pin	$-3$ —	— $+3$	mA	1
	• $V_{IN} < V_{SS}-0.3\text{V}$ (Negative current injection)				
	• $V_{IN} > V_{DD}+0.3\text{V}$ (Positive current injection)				
$I_{ICcont}$	Contiguous pin DC injection current —regional limit, includes sum of negative injection currents or sum of positive injection currents of 16 contiguous pins	$-25$ —	— $+25$	mA	1
	• Negative current injection				
	• Positive current injection				
$V_{RAM}$	$V_{DD}$ voltage required to retain RAM	1.2	—	V	
$V_{RFVBAT}$	$V_{BAT}$ voltage required to retain the VBAT register file	$V_{POR\_VBAT}$	—	V	

1. All analog pins are internally clamped to  $V_{SS}$  and  $V_{DD}$  through ESD protection diodes. If  $V_{IN}$  is greater than  $V_{AIO\_MIN}$  ( $=V_{SS}-0.3\text{V}$ ) and  $V_{IN}$  is less than  $V_{AIO\_MAX}$  ( $=V_{DD}+0.3\text{V}$ ) is observed, then there is no need to provide current limiting resistors at the pads. If these limits cannot be observed then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as  $R=(V_{AIO\_MIN}-V_{IN})/I_{ICl}$ . The positive injection current limiting resistor is calculated as  $R=(V_{IN}-V_{AIO\_MAX})/I_{ICl}$ . Select the larger of these two calculated resistances.

## 5.2.2 LVD and POR operating requirements

**Table 2. V<sub>DD</sub> supply LVD and POR operating requirements**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V <sub>POR</sub>	Falling VDD POR detect voltage	0.8	1.1	1.5	V	
V <sub>LVDH</sub>	Falling low-voltage detect threshold — high range (LVDV=01)	2.48	2.56	2.64	V	
V <sub>LVW1H</sub>	Low-voltage warning thresholds — high range					1
	• Level 1 falling (LVWV=00)	2.62	2.70	2.78	V	
V <sub>LVW2H</sub>	• Level 2 falling (LVWV=01)	2.72	2.80	2.88	V	
V <sub>LVW3H</sub>	• Level 3 falling (LVWV=10)	2.82	2.90	2.98	V	
V <sub>LVW4H</sub>	• Level 4 falling (LVWV=11)	2.92	3.00	3.08	V	
V <sub>HYSH</sub>	Low-voltage inhibit reset/recover hysteresis — high range	—	±80	—	mV	
V <sub>LVDL</sub>	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	
V <sub>LVW1L</sub>	Low-voltage warning thresholds — low range					1
	• Level 1 falling (LVWV=00)	1.74	1.80	1.86	V	
V <sub>LVW2L</sub>	• Level 2 falling (LVWV=01)	1.84	1.90	1.96	V	
V <sub>LVW3L</sub>	• Level 3 falling (LVWV=10)	1.94	2.00	2.06	V	
V <sub>LVW4L</sub>	• Level 4 falling (LVWV=11)	2.04	2.10	2.16	V	
V <sub>HYSL</sub>	Low-voltage inhibit reset/recover hysteresis — low range	—	±60	—	mV	
V <sub>BG</sub>	Bandgap voltage reference	0.97	1.00	1.03	V	
t <sub>LPO</sub>	Internal low power oscillator period — factory trimmed	900	1000	1100	μs	

1. Rising thresholds are falling threshold + hysteresis voltage

**Table 3. VBAT power operating requirements**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V <sub>POR_VBAT</sub>	Falling VBAT supply POR detect voltage	0.8	1.1	1.5	V	

### 5.2.3 Voltage and current operating behaviors

Table 4. Voltage and current operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
$V_{OH}$	Output high voltage — high drive strength • $2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$ , $I_{OH} = -9 \text{ mA}$	$V_{DD} - 0.5$	—	V	
	• $1.71 \text{ V} \leq V_{DD} \leq 2.7 \text{ V}$ , $I_{OH} = -3 \text{ mA}$	$V_{DD} - 0.5$	—	V	
$V_{OL}$	Output low voltage — high drive strength • $2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$ , $I_{OL} = 9 \text{ mA}$	—	0.5	V	
	• $1.71 \text{ V} \leq V_{DD} \leq 2.7 \text{ V}$ , $I_{OL} = 3 \text{ mA}$	—	0.5	V	
$I_{OHT}$	Output high current total for all ports	—	100	mA	
$I_{OLT}$	Output low voltage — low drive strength • $2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$ , $I_{OL} = 2 \text{ mA}$	—	0.5	V	
	• $1.71 \text{ V} \leq V_{DD} \leq 2.7 \text{ V}$ , $I_{OL} = 0.6 \text{ mA}$	—	0.5	V	
$I_{OLT}$	Output low current total for all ports	—	100	mA	
$I_{IN}$	Input leakage current (per pin) • @ full temperature range	—	1.0	$\mu\text{A}$	1
	• @ $25^\circ\text{C}$	—	0.1	$\mu\text{A}$	
$I_{OZ}$	Hi-Z (off-state) leakage current (per pin)	—	1	$\mu\text{A}$	
$I_{OZ}$	Total Hi-Z (off-state) leakage current (all input pins)	—	4	$\mu\text{A}$	
$R_{PU}$	Internal pullup resistors	22	50	k $\Omega$	2
$R_{PD}$	Internal pulldown resistors	22	50	k $\Omega$	3

1. Tested by ganged leakage method

2. Measured at  $V_{input} = V_{SS}$

3. Measured at  $V_{input} = V_{DD}$

### 5.2.4 Power mode transition operating behaviors

All specifications except  $t_{POR}$ , and  $VLLSx \rightarrow RUN$  recovery times in the following table assume this clock configuration:

- CPU and system clocks = 50 MHz
- Bus clock = 50 MHz
- Flash clock = 25 MHz

**Table 5. Power mode transition operating behaviors**

Symbol	Description	Min.	Max.	Unit	Notes
$t_{POR}$	After a POR event, amount of time from the point $V_{DD}$ reaches 1.71 V to execution of the first instruction across the operating temperature range of the chip.	—	300	μs	1
	• VLLS0 → RUN	—	130	μs	
	• VLLS1 → RUN	—	130	μs	
	• VLLS2 → RUN	—	75	μs	
	• VLLS3 → RUN	—	75	μs	
	• LLS → RUN	—	6.2	μs	
	• VLPS → RUN	—	5.8	μs	
	• STOP → RUN	—	TBD	μs	

1. Normal boot (FTFL\_OPT[LPBOOT]=1)

## 5.2.5 Power consumption operating behaviors

**Table 6. Power consumption operating behaviors**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$I_{DDA}$	Analog supply current	—	—	See note	mA	1
$I_{DD\_RUN}$	Run mode current — all peripheral clocks disabled, code executing from flash					2
	• @ 1.8V	—	13.7	TBD	mA	
	• @ 3.0V	—	13.9	TBD	mA	
$I_{DD\_RUN}$	Run mode current — all peripheral clocks enabled, code executing from flash					3, 4
	• @ 1.8V	—	16.6	TBD	mA	
	• @ 3.0V		16.8	TBD	mA	
	• @ 25°C	—	17.2	TBD	mA	
	• @ 125°C	—				
$I_{DD\_WAIT}$	Wait mode high frequency current at 3.0 V — all peripheral clocks disabled	—	7.5	TBD	mA	2
$I_{DD\_WAIT}$	Wait mode reduced frequency current at 3.0 V — all peripheral clocks disabled	—	5.6	TBD	mA	5
$I_{DD\_STOP}$	Stop mode current at 3.0 V	—	318	TBD	μA	

Table continues on the next page...

**Table 6. Power consumption operating behaviors (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I <sub>DD_VLPR</sub>	Very-low-power run mode current at 3.0 V — all peripheral clocks disabled	—	556	TBD	µA	6
I <sub>DD_VLPR</sub>	Very-low-power run mode current at 3.0 V — all peripheral clocks enabled	—	0.67	TBD	mA	7
I <sub>DD_VLPW</sub>	Very-low-power wait mode current at 3.0 V	—	339	TBD	µA	8
I <sub>DD_VLPS</sub>	Very-low-power stop mode current at 3.0 V	—	3.6	TBD	µA	
I <sub>DD_LLSS</sub>	Low leakage stop mode current at 3.0 V	—	2.2	TBD	µA	
I <sub>DD_VLLS3</sub>	Very low-leakage stop mode 3 current at 3.0 V	—	1.58	TBD	µA	
I <sub>DD_VLLS2</sub>	Very low-leakage stop mode 2 current at 3.0 V	—	1.5	TBD	µA	
I <sub>DD_VLLS1</sub>	Very low-leakage stop mode 1 current at 3.0 V	—	748	TBD	nA	
I <sub>DD_VLLS0</sub>	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit enabled	—	414	TBD	nA	
I <sub>DD_VLLS0</sub>	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit disabled	—	222	TBD	nA	
I <sub>DD_VBAT</sub>	Average current when CPU is not accessing RTC registers  • @ 1.8V • @ -40 to 25°C • @ 70°C • @ 105°C • @ 3.0V • @ -40 to 25°C • @ 70°C • @ 105°C	— — — — — — — — — — — — — — —	TBD TBD TBD 0.67 1.1 2.7	TBD TBD TBD 0.83 1.45 3.8	µA µA µA µA µA µA	9

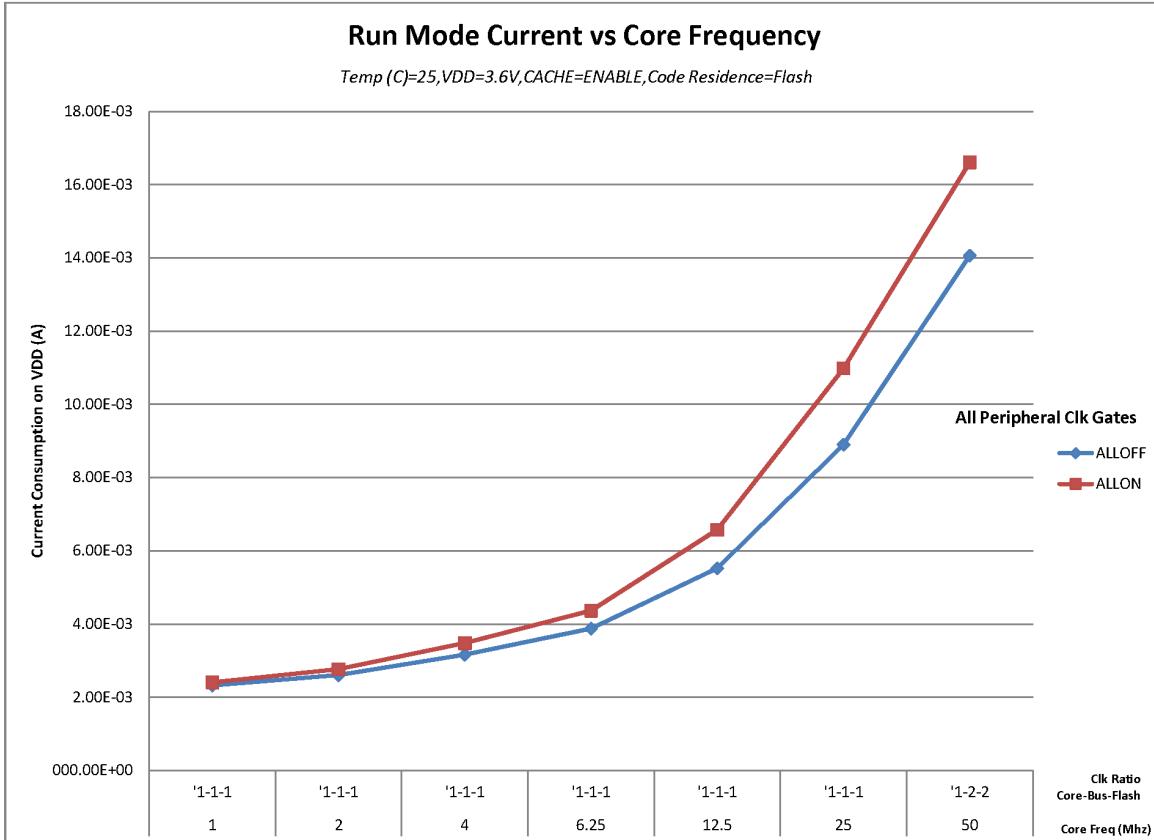
1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
  2. 50MHz core and system clock, 25MHz bus clock, and 25MHz flash clock . MCG configured for FEI mode. All peripheral clocks disabled.
  3. 50MHz core and system clock, 25MHz bus clock, and 25MHz flash clock. MCG configured for FEI mode. All peripheral clocks enabled, and peripherals are in active operation.
  4. Max values are measured with CPU executing DSP instructions
  5. 25MHz core and system clock, 25MHz bus clock, and 12.5MHz flash clock. MCG configured for FEI mode.
  6. 2 MHz core, system, and bus clock and 1MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled. Code executing from flash.
  7. 2 MHz core, system, and bus clock and 1MHz flash clock. MCG configured for BLPE mode. All peripheral clocks enabled but peripherals are not in active operation. Code executing from flash.
  8. 2 MHz core, system, and bus clock and 1MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled.
  9. Includes 32kHz oscillator current and RTC operation.

### 5.2.5.1 Diagram: Typical IDD RUN operating behavior

The following data was measured under these conditions:

## General

- MCG in FBE mode
- USB regulator disabled
- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFL



**Figure 2. Run mode supply current vs. core frequency**

## 5.2.6 EMC radiated emissions operating behaviors

Table 7. EMC radiated emissions operating behaviors for 64LQFP

Symbol	Description	Frequency band (MHz)	Typ.	Unit	Notes
$V_{RE1}$	Radiated emissions voltage, band 1	0.15–50	TBD	$\text{dB}\mu\text{V}$	1
$V_{RE2}$	Radiated emissions voltage, band 2	50–150	TBD	$\text{dB}\mu\text{V}$	
$V_{RE3}$	Radiated emissions voltage, band 3	150–500	TBD	$\text{dB}\mu\text{V}$	
$V_{RE4}$	Radiated emissions voltage, band 4	500–1000	TBD	$\text{dB}\mu\text{V}$	
$V_{RE\_IEC}$	IEC level	0.15–1000	K	—	2

1. Determined according to IEC Standard 61967-1, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions* and IEC Standard 61967-2, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*. Measurements were made while the microcontroller was running basic application code. The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.
2. Specified according to Annex D of IEC Standard 61967-2, *Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*

## 5.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to <http://www.freescale.com>.
2. Perform a keyword search for “EMC design.”

## 5.2.8 Capacitance attributes

Table 8. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
$C_{IN\_A}$	Input capacitance: analog pins	—	7	pF
$C_{IN\_D}$	Input capacitance: digital pins	—	7	pF

## 5.3 Switching specifications

### 5.3.1 Device clock specifications

**Table 9. Device clock specifications**

Symbol	Description	Min.	Max.	Unit	Notes
Normal run mode					
$f_{SYS}$	System and core clock	—	50	MHz	
$f_{SYS\_USB}$	System and core clock when Full Speed USB in operation	20	—	MHz	
$f_{BUS}$	Bus clock	—	50	MHz	
$f_{FLASH}$	Flash clock	—	25	MHz	
$f_{LPTMR}$	LPTMR clock	—	25	MHz	
VLPR mode <sup>1</sup>					
$f_{SYS}$	System and core clock	—	4	MHz	
$f_{BUS}$	Bus clock	—	4	MHz	
$f_{FLASH}$	Flash clock	—	1	MHz	
$f_{ERCLK}$	External reference clock	—	16	MHz	
$f_{LPTMR\_pin}$	LPTMR clock	—	25	MHz	
$f_{LPTMR\_ERCLK}$	LPTMR external reference clock	—	16	MHz	
$f_{I2S\_MCLK}$	I2S master clock	—	12.5	MHz	
$f_{I2S\_BCLK}$	I2S bit clock	—	4	MHz	

1. The frequency limitations in VLPR mode here override any frequency specification listed in the timing specification for any other module.

### 5.3.2 General switching specifications

These general purpose specifications apply to all signals configured for GPIO, UART, CMT, and I<sup>2</sup>C signals.

**Table 10. General switching specifications**

Symbol	Description	Min.	Max.	Unit	Notes
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	<sup>1</sup>
	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter enabled) — Asynchronous path	100	—	ns	<sup>2</sup>
	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter disabled) — Asynchronous path	50	—	ns	<sup>2</sup>
	External reset pulse width (digital glitch filter disabled)	100	—	ns	<sup>2</sup>
	Mode select (EZP_CS) hold time after reset deassertion	2	—	Bus clock cycles	

*Table continues on the next page...*

**Table 10. General switching specifications (continued)**

Symbol	Description	Min.	Max.	Unit	Notes
	Port rise and fall time (high drive strength) <ul style="list-style-type: none"> <li>Slew disabled               <ul style="list-style-type: none"> <li><math>1.71 \leq V_{DD} \leq 2.7V</math></li> <li><math>2.7 \leq V_{DD} \leq 3.6V</math></li> </ul> </li> <li>Slew enabled               <ul style="list-style-type: none"> <li><math>1.71 \leq V_{DD} \leq 2.7V</math></li> <li><math>2.7 \leq V_{DD} \leq 3.6V</math></li> </ul> </li> </ul>	— — — — —	13 7 36 24	ns ns ns ns	3
	Port rise and fall time (low drive strength) <ul style="list-style-type: none"> <li>Slew disabled               <ul style="list-style-type: none"> <li><math>1.71 \leq V_{DD} \leq 2.7V</math></li> <li><math>2.7 \leq V_{DD} \leq 3.6V</math></li> </ul> </li> <li>Slew enabled               <ul style="list-style-type: none"> <li><math>1.71 \leq V_{DD} \leq 2.7V</math></li> <li><math>2.7 \leq V_{DD} \leq 3.6V</math></li> </ul> </li> </ul>	— — — — —	12 6 36 24	ns ns ns ns	4

1. The greater synchronous and asynchronous timing must be met.
2. This is the shortest pulse that is guaranteed to be recognized.
3. 75pF load
4. 15pF load

## 5.4 Thermal specifications

### 5.4.1 Thermal operating requirements

**Table 11. Thermal operating requirements**

Symbol	Description	Min.	Max.	Unit
$T_J$	Die junction temperature	-40	125	°C
$T_A$	Ambient temperature	-40	105	°C

## 5.4.2 Thermal attributes

Board type	Symbol	Description	Package TBD	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	TBD	°C/W	
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	TBD	°C/W	
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	TBD	°C/W	
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	TBD	°C/W	
—	$R_{\theta JB}$	Thermal resistance, junction to board	TBD	°C/W	1
—	$R_{\theta JC}$	Thermal resistance, junction to case	TBD	°C/W	2
—	$\Psi_{JT}$	Thermal characterization parameter, junction to package top outside center (natural convection)	TBD	°C/W	3

1. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*.
2. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
3. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.

## 6 Peripheral operating requirements and behaviors

### 6.1 Core modules

## 6.1.1 JTAG electricals

**Table 12. JTAG limited voltage range electricals**

Symbol	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
J1	TCLK frequency of operation <ul style="list-style-type: none"> <li>• Boundary Scan</li> <li>• JTAG and CJTAG</li> <li>• Serial Wire Debug</li> </ul>	0	10	MHz
		0	25	
		0	50	
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width <ul style="list-style-type: none"> <li>• Boundary Scan</li> <li>• JTAG and CJTAG</li> <li>• Serial Wire Debug</li> </ul>	50	—	ns
		20	—	ns
		10	—	ns
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	0	—	ns
J7	TCLK low to boundary scan output data valid	—	25	ns
J8	TCLK low to boundary scan output high-Z	—	25	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1	—	ns
J11	TCLK low to TDO data valid	—	17	ns
J12	TCLK low to TDO high-Z	—	17	ns
J13	TRST assert time	100	—	ns
J14	TRST setup time (negation) to TCLK high	8	—	ns

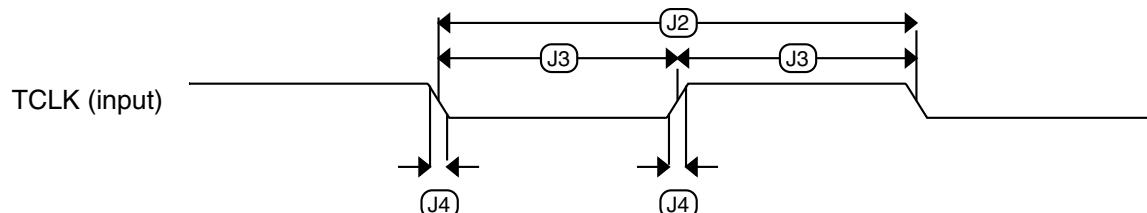
**Table 13. JTAG full voltage range electricals**

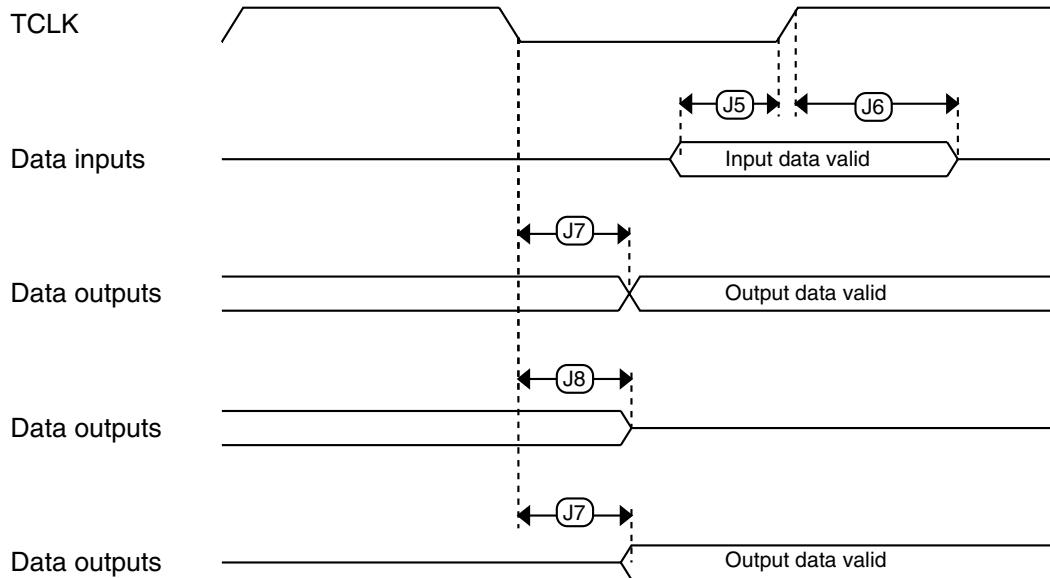
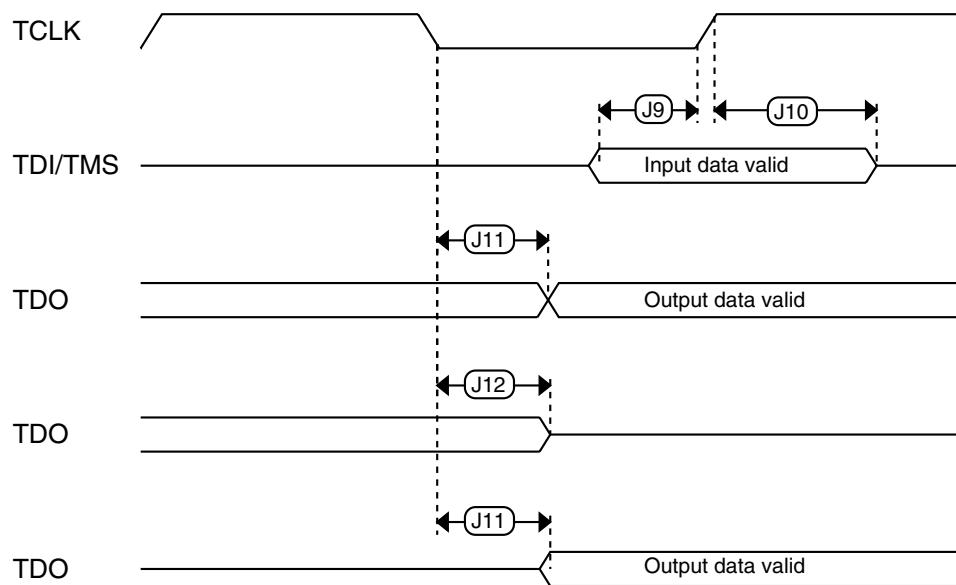
Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
J1	TCLK frequency of operation <ul style="list-style-type: none"> <li>• Boundary Scan</li> <li>• JTAG and CJTAG</li> <li>• Serial Wire Debug</li> </ul>	0	10	MHz
		0	20	
		0	40	
J2	TCLK cycle period	1/J1	—	ns

*Table continues on the next page...*

**Table 13. JTAG full voltage range electricals (continued)**

Symbol	Description	Min.	Max.	Unit
J3	TCLK clock pulse width			
	• Boundary Scan	50	—	ns
	• JTAG and CJTAG	25	—	ns
	• Serial Wire Debug	12.5	—	ns
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	0	—	ns
J7	TCLK low to boundary scan output data valid	—	25	ns
J8	TCLK low to boundary scan output high-Z	—	25	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1.4	—	ns
J11	TCLK low to TDO data valid	—	22.1	ns
J12	TCLK low to TDO high-Z	—	22.1	ns
J13	TRST assert time	100	—	ns
J14	TRST setup time (negation) to TCLK high	8	—	ns

**Figure 3. Test clock input timing**

**Figure 4. Boundary scan (JTAG) timing****Figure 5. Test Access Port timing**

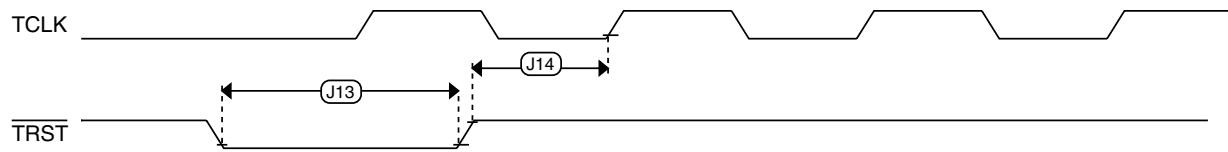


Figure 6. TRST timing

## 6.2 System modules

There are no specifications necessary for the device's system modules.

## 6.3 Clock modules

### 6.3.1 MCG specifications

Table 14. MCG specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$f_{ints\_ft}$	Internal reference frequency (slow clock) — factory trimmed at nominal VDD and 25 °C	—	32.768	—	kHz	
$f_{ints\_t}$	Internal reference frequency (slow clock) — user trimmed	31.25	—	39.0625	kHz	
$I_{ints}$	Internal reference (slow clock) current	—	TBD	—	µA	
$\Delta f_{dco\_res\_t}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM and SCFTRIM	—	± 0.3	± 0.6	% $f_{dco}$	1
$\Delta f_{dco\_t}$	Total deviation of trimmed average DCO output frequency over voltage and temperature	—	± 1.5	—	% $f_{dco}$	1
$\Delta f_{dco\_v}$	Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0–70°C	—	± 1.0	TBD	% $f_{dco}$	1
$f_{intf\_ft}$	Internal reference frequency (fast clock) — factory trimmed at nominal VDD and 25°C			4	MHz	
$f_{intf\_t}$	Internal reference frequency (fast clock) — user trimmed at nominal VDD and 25 °C	3	—	5	MHz	
$I_{intf}$	Internal reference (fast clock) current	—	TBD	—	µA	
$f_{loc\_low}$	Loss of external clock minimum frequency — RANGE = 00	(3/5) × $f_{ints\_t}$	—	—	kHz	

Table continues on the next page...

**Table 14. MCG specifications (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$f_{loc\_high}$	Loss of external clock minimum frequency — RANGE = 01, 10, or 11	(16/5) × $f_{ints\_t}$	—	—	kHz	
FLL						
$f_{fll\_ref}$	FLL reference frequency range	31.25	—	39.0625	kHz	
$f_{dco}$	DCO output frequency range	Low range (DRS=00) $640 \times f_{fll\_ref}$	20	20.97	25	MHz
		Mid range (DRS=01) $1280 \times f_{fll\_ref}$	40	41.94	50	MHz
		Mid-high range (DRS=10) $1920 \times f_{fll\_ref}$	60	62.91	75	MHz
		High range (DRS=11) $2560 \times f_{fll\_ref}$	80	83.89	100	MHz
$f_{dco\_t\_DMX3\_2}$	DCO output frequency	Low range (DRS=00) $732 \times f_{fll\_ref}$	—	23.99	—	MHz
		Mid range (DRS=01) $1464 \times f_{fll\_ref}$	—	47.97	—	MHz
		Mid-high range (DRS=10) $2197 \times f_{fll\_ref}$	—	71.99	—	MHz
		High range (DRS=11) $2929 \times f_{fll\_ref}$	—	95.98	—	MHz
$J_{cyc\_fll}$	FLL period jitter • $f_{VCO} = 48$ MHz • $f_{VCO} = 98$ MHz	—	180	—	ps	
		—	150	—	ps	
$t_{fll\_acquire}$	FLL target frequency acquisition time	—	—	1	ms	6
PLL						
$f_{vco}$	VCO operating frequency	48.0	—	100	MHz	
$I_{pll}$	PLL operating current • PLL @ 96 MHz ( $f_{osc\_hi\_1} = 8$ MHz, $f_{pll\_ref} = 2$ MHz, VDIV multiplier = 48)	—	1060	—	μA	7
$I_{pll}$	PLL operating current • PLL @ 48 MHz ( $f_{osc\_hi\_1} = 8$ MHz, $f_{pll\_ref} = 2$ MHz, VDIV multiplier = 24)	—	600	—	μA	7
$f_{pll\_ref}$	PLL reference frequency range	2.0	—	4.0	MHz	
$J_{cyc\_pll}$	PLL period jitter (RMS) • $f_{VCO} = 48$ MHz • $f_{VCO} = 100$ MHz	—	120	—	ps	
		—	50	—	ps	

Table continues on the next page...

**Table 14. MCG specifications (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
J <sub>acc_pll</sub>	PLL accumulated jitter over 1μs (RMS) <ul style="list-style-type: none"> <li>• f<sub>VCO</sub> = 48 MHz</li> <li>• f<sub>VCO</sub> = 100 MHz</li> </ul>	—	1350	—	ps	8
D <sub>lock</sub>	Lock entry frequency tolerance	± 1.49	—	± 2.98	%	
D <sub>unl</sub>	Lock exit frequency tolerance	± 4.47	—	± 5.97	%	
t <sub>pll_lock</sub>	Lock detector detection time	—	—	150 × 10 <sup>-6</sup> + 1075(1/ f <sub>pll_ref</sub> )	s	9

1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
2. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=0.
3. The resulting system clock frequencies should not exceed their maximum specified values. The DCO frequency deviation ( $\Delta f_{dcos_t}$ ) over voltage and temperature should be considered.
4. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=1.
5. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
6. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
7. Excludes any oscillator currents that are also consuming power while PLL is in operation.
8. This specification was obtained using a Freescale developed PCB. PLL jitter is dependent on the noise characteristics of each PCB and results will vary.
9. This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

### 6.3.2 Oscillator electrical specifications

This section provides the electrical characteristics of the module.

#### 6.3.2.1 Oscillator DC electrical specifications

**Table 15. Oscillator DC electrical specifications**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V <sub>DD</sub>	Supply voltage	1.71	—	3.6	V	
I <sub>DDOSC</sub>	Supply current — low-power mode (HGO=0) <ul style="list-style-type: none"> <li>• 32 kHz</li> <li>• 4 MHz</li> <li>• 8 MHz (RANGE=01)</li> <li>• 16 MHz</li> <li>• 24 MHz</li> <li>• 32 MHz</li> </ul>	—	500	—	nA	1
		—	200	—	μA	
		—	300	—	μA	
		—	950	—	μA	
		—	1.2	—	mA	
		—	1.5	—	mA	

Table continues on the next page...

**Table 15. Oscillator DC electrical specifications (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$I_{DDOSC}$	Supply current — high gain mode (HGO=1) <ul style="list-style-type: none"> <li>• 32 kHz</li> <li>• 4 MHz</li> <li>• 8 MHz (RANGE=01)</li> <li>• 16 MHz</li> <li>• 24 MHz</li> <li>• 32 MHz</li> </ul>	—	25	—	μA	1
		—	400	—	μA	
		—	500	—	μA	
		—	2.5	—	mA	
		—	3	—	mA	
		—	4	—	mA	
$C_x$	EXTAL load capacitance	—	—	—		2, 3
$C_y$	XTAL load capacitance	—	—	—		2, 3
$R_F$	Feedback resistor — low-frequency, low-power mode (HGO=0)	—	—	—	MΩ	2, 4
	Feedback resistor — low-frequency, high-gain mode (HGO=1)	—	10	—	MΩ	
	Feedback resistor — high-frequency, low-power mode (HGO=0)	—	—	—	MΩ	
	Feedback resistor — high-frequency, high-gain mode (HGO=1)	—	1	—	MΩ	
$R_S$	Series resistor — low-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — low-frequency, high-gain mode (HGO=1)	—	200	—	kΩ	
	Series resistor — high-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — high-frequency, high-gain mode (HGO=1)	—	0	—	kΩ	
$V_{pp}^5$	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1)	—	$V_{DD}$	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1)	—	$V_{DD}$	—	V	

1.  $V_{DD}=3.3$  V, Temperature =25 °C
2. See crystal or resonator manufacturer's recommendation
3.  $C_x, C_y$  can be provided by using either the integrated capacitors or by using external components.
4. When low power mode is selected,  $R_F$  is integrated and must not be attached externally.

## Peripheral operating requirements and behaviors

- The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.

### 6.3.2.2 Oscillator frequency specifications

Table 16. Oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$f_{osc\_lo}$	Oscillator crystal or resonator frequency — low frequency mode (MCG_C2[RANGE]=00)	32	—	40	kHz	
$f_{osc\_hi\_1}$	Oscillator crystal or resonator frequency — high frequency mode (low range) (MCG_C2[RANGE]=01)	3	—	8	MHz	
$f_{osc\_hi\_2}$	Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x)	8	—	32	MHz	
$f_{ec\_extal}$	Input clock frequency (external clock mode)	—	—	50	MHz	1, 2
$t_{dc\_extal}$	Input clock duty cycle (external clock mode)	40	50	60	%	
$t_{cst}$	Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0)	—	750	—	ms	3, 4
	Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1)	—	250	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), low-power mode (HGO=0)	—	0.6	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), high-gain mode (HGO=1)	—	1	—	ms	

- Other frequency limits may apply when external clock is being used as a reference for the FLL or PLL.
- When transitioning from FBE to FEI mode, restrict the frequency of the input clock so that, when it is divided by FRDIV, it remains within the limits of the DCO input clock frequency.
- Proper PC board layout procedures must be followed to achieve specifications.
- Crystal startup time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG\_S register being set.

### 6.3.3 32kHz Oscillator Electrical Characteristics

This section describes the module electrical characteristics.

#### 6.3.3.1 32kHz oscillator DC electrical specifications

Table 17. 32kHz oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
$V_{BAT}$	Supply voltage	1.71	—	3.6	V
$R_F$	Internal feedback resistor	—	100	—	$\text{M}\Omega$

Table continues on the next page...

**Table 17. 32kHz oscillator DC electrical specifications (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit
$C_{\text{para}}$	Parasitical capacitance of EXTAL32 and XTAL32	—	5	7	pF
$V_{\text{pp}}^{\text{1}}$	Peak-to-peak amplitude of oscillation	—	0.6	—	V

1. The EXTAL32 and XTAL32 pins should only be connected to required oscillator components and must not be connected to any other devices.

### 6.3.3.2 32kHz oscillator frequency specifications

**Table 18. 32kHz oscillator frequency specifications**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$f_{\text{osc\_lo}}$	Oscillator crystal	—	32.768	—	kHz	
$t_{\text{start}}$	Crystal start-up time	—	1000	—	ms	<b>1</b>

1. Proper PC board layout procedures must be followed to achieve specifications.

## 6.4 Memories and memory interfaces

### 6.4.1 Flash (FTFL) electrical specifications

This section describes the electrical characteristics of the FTFL module.

#### 6.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

**Table 19. NVM program/erase timing specifications**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{\text{hvpgm4}}$	Longword Program high-voltage time	—	7.5	18	μs	
$t_{\text{hversscr}}$	Sector Erase high-voltage time	—	13	113	ms	<b>1</b>
$t_{\text{hversblk32k}}$	Erase Block high-voltage time for 32 KB	—	52	452	ms	<b>1</b>
$t_{\text{hversblk128k}}$	Erase Block high-voltage time for 128 KB	—	52	452	ms	<b>1</b>

1. Maximum time based on expectations at cycling end-of-life.

## 6.4.1.2 Flash timing specifications — commands

Table 20. Flash command timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{rd1blk32k}$	Read 1s Block execution time • 32 KB data flash	—	—	0.5	ms	
$t_{rd1blk128k}$	• 128 KB program flash	—	—	1.7	ms	
$t_{rd1sec1k}$	Read 1s Section execution time (data flash sector)	—	—	60	μs	1
$t_{pgmchk}$	Program Check execution time	—	—	45	μs	1
$t_{drsrc}$	Read Resource execution time	—	—	30	μs	1
$t_{pgm4}$	Program Longword execution time	—	65	145	μs	
$t_{ersblk32k}$	Erase Flash Block execution time • 32 KB data flash	—	55	465	ms	2
$t_{ersblk128k}$	• 128 KB program flash	—	61	495	ms	
$t_{ersscr}$	Erase Flash Sector execution time	—	14	114	ms	2
$t_{pgmsec512}$	Program Section execution time • 512 B flash	—	4.7	—	ms	
$t_{pgmsec1k}$	• 1 KB flash	—	9.3	—	ms	
$t_{rd1all}$	Read 1s All Blocks execution time	—	—	1.8	ms	
$t_{rdonce}$	Read Once execution time	—	—	25	μs	1
$t_{pgmonce}$	Program Once execution time	—	65	—	μs	
$t_{ersall}$	Erase All Blocks execution time	—	115	1000	ms	2
$t_{vfykey}$	Verify Backdoor Access Key execution time	—	—	30	μs	1
$t_{pgmpart32k}$	Program Partition for EEPROM execution time • 32 KB FlexNVM	—	70	—	ms	
$t_{setramff}$	Set FlexRAM Function execution time: • Control Code 0xFF	—	50	—	μs	
$t_{setram8k}$	• 8 KB EEPROM backup	—	0.3	0.5	ms	
$t_{setram32k}$	• 32 KB EEPROM backup	—	0.7	1.0	ms	
Byte-write to FlexRAM for EEPROM operation						
$t_{eewr8bers}$	Byte-write to erased FlexRAM location execution time	—	175	260	μs	3
$t_{eewr8b8k}$	Byte-write to FlexRAM execution time: • 8 KB EEPROM backup	—	340	1700	μs	
$t_{eewr8b16k}$	• 16 KB EEPROM backup	—	385	1800	μs	
$t_{eewr8b32k}$	• 32 KB EEPROM backup	—	475	2000	μs	

Table continues on the next page...

**Table 20. Flash command timing specifications (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
Word-write to FlexRAM for EEPROM operation						
$t_{eewr16bers}$	Word-write to erased FlexRAM location execution time	—	175	260	μs	
$t_{eewr16b8k}$	Word-write to FlexRAM execution time:	—	340	1700	μs	
$t_{eewr16b16k}$	• 8 KB EEPROM backup	—	385	1800	μs	
$t_{eewr16b32k}$	• 16 KB EEPROM backup	—	475	2000	μs	
Longword-write to FlexRAM for EEPROM operation						
$t_{eewr32bers}$	Longword-write to erased FlexRAM location execution time	—	360	540	μs	
$t_{eewr32b8k}$	Longword-write to FlexRAM execution time:	—	545	1950	μs	
$t_{eewr32b16k}$	• 8 KB EEPROM backup	—	630	2050	μs	
$t_{eewr32b32k}$	• 16 KB EEPROM backup	—	810	2250	μs	

- Assumes 25MHz flash clock frequency.
- Maximum times for erase parameters based on expectations at cycling end-of-life.
- For byte-writes to an erased FlexRAM location, the aligned word containing the byte must be erased.

#### 6.4.1.3 Flash (FTFL) current and power specifications

**Table 21. Flash (FTFL) current and power specifications**

Symbol	Description	Typ.	Unit
$I_{DD\_PGM}$	Worst case programming current in program flash	10	mA

#### 6.4.1.4 Reliability specifications

**Table 22. NVM reliability specifications**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
Program Flash						
$t_{nvmret10k}$	Data retention after up to 10 K cycles	5	50	—	years	<a href="#">2</a>
$t_{nvmret1k}$	Data retention after up to 1 K cycles	10	100	—	years	<a href="#">2</a>
$t_{nvmret100}$	Data retention after up to 100 cycles	15	100	—	years	<a href="#">2</a>
$n_{nvmcycp}$	Cycling endurance	10 K	35 K	—	cycles	<a href="#">3</a>
Data Flash						
$t_{nvmretd10k}$	Data retention after up to 10 K cycles	5	50	—	years	<a href="#">2</a>
$t_{nvmretd1k}$	Data retention after up to 1 K cycles	10	100	—	years	<a href="#">2</a>

Table continues on the next page...

**Table 22. NVM reliability specifications (continued)**

Symbol	Description	Min.	Typ. <sup>1</sup>	Max.	Unit	Notes
$t_{\text{nvmretd}100}$	Data retention after up to 100 cycles	15	100	—	years	<b>2</b>
$n_{\text{nvmcycd}}$	Cycling endurance	10 K	35 K	—	cycles	<b>3</b>
FlexRAM as EEPROM						
$t_{\text{nvmretee}100}$	Data retention up to 100% of write endurance	5	50	—	years	<b>2</b>
$t_{\text{nvmretee}10}$	Data retention up to 10% of write endurance	10	100	—	years	<b>2</b>
$t_{\text{nvmretee}1}$	Data retention up to 1% of write endurance	15	100	—	years	<b>2</b>
$n_{\text{nvmwree}16}$ $n_{\text{nvmwree}128}$ $n_{\text{nvmwree}512}$ $n_{\text{nvmwree}4k}$ $n_{\text{nvmwree}8k}$	Write endurance • EEPROM backup to FlexRAM ratio = 16 • EEPROM backup to FlexRAM ratio = 128 • EEPROM backup to FlexRAM ratio = 512 • EEPROM backup to FlexRAM ratio = 4096 • EEPROM backup to FlexRAM ratio = 8192	35 K 315 K 1.27 M 10 M 20 M	175 K 1.6 M 6.4 M 50 M 100 M	— — — — —	writes writes writes writes writes	<b>4</b>

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25°C use profile. Engineering Bulletin EB618 does not apply to this technology.
2. Data retention is based on  $T_{\text{avg}} = 55^{\circ}\text{C}$  (temperature profile over the lifetime of the application).
3. Cycling endurance represents number of program/erase cycles at  $-40^{\circ}\text{C} \leq T_j \leq 125^{\circ}\text{C}$ .
4. Write endurance represents the number of writes to each FlexRAM location at  $-40^{\circ}\text{C} \leq T_j \leq 125^{\circ}\text{C}$  influenced by the cycling endurance of the FlexNVM (same value as data flash) and the allocated EEPROM backup. Minimum and typical values assume all byte-writes to FlexRAM.

#### 6.4.1.5 Write endurance to FlexRAM for EEPROM

When the FlexNVM partition code is not set to full data flash, the EEPROM data set size can be set to any of several non-zero values.

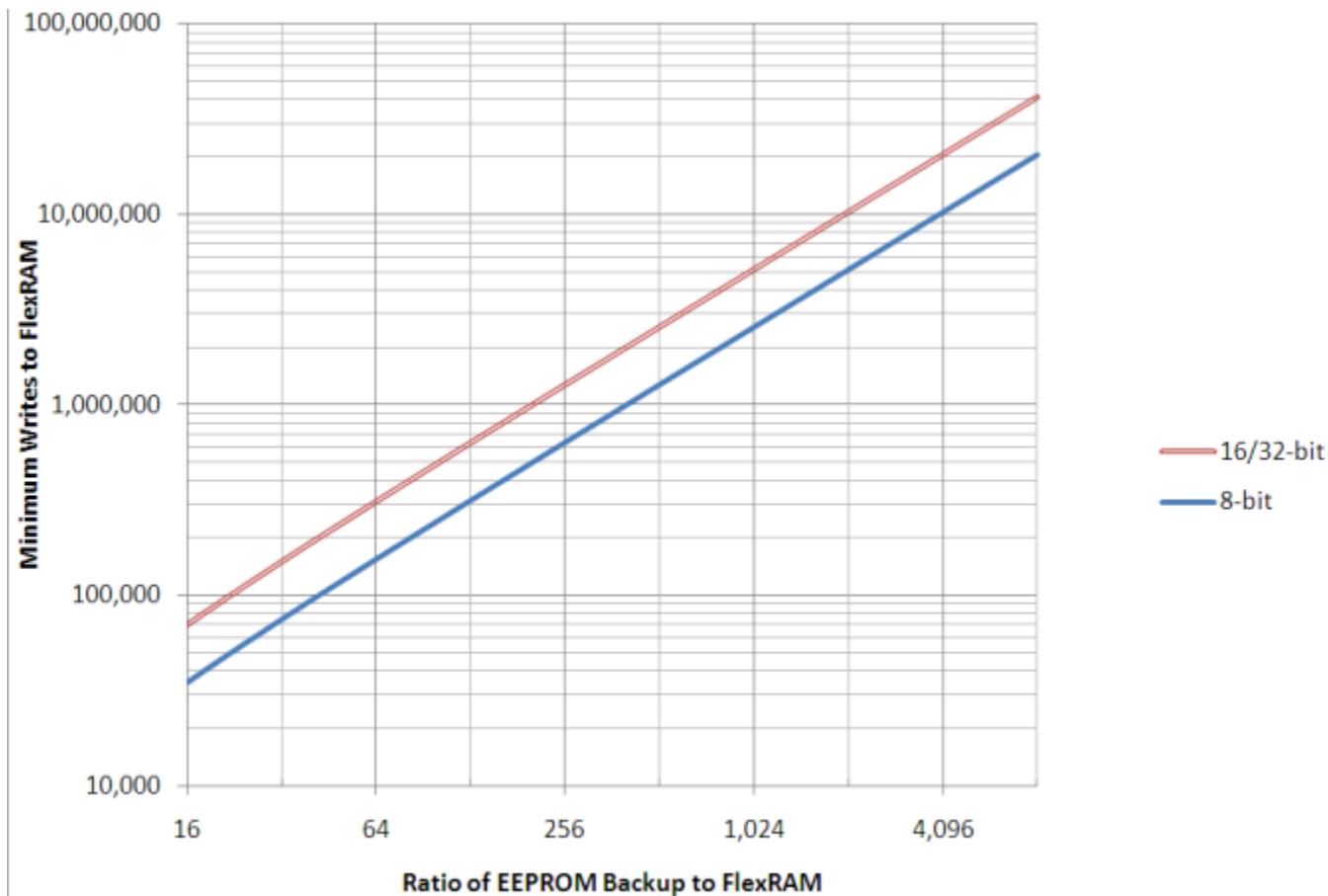
The bytes not assigned to data flash via the FlexNVM partition code are used by the FTFL to obtain an effective endurance increase for the EEPROM data. The built-in EEPROM record management system raises the number of program/erase cycles that can be attained prior to device wear-out by cycling the EEPROM data through a larger EEPROM NVM storage space.

While different partitions of the FlexNVM are available, the intention is that a single choice for the FlexNVM partition code and EEPROM data set size is used throughout the entire lifetime of a given application. The EEPROM endurance equation and graph shown below assume that only one configuration is ever used.

$$\text{Writes_FlexRAM} = \frac{\text{EEPROM} - 2 \times \text{EEESIZE}}{\text{EEESIZE}} \times \text{Write_efficiency} \times n_{\text{nvmcycd}}$$

where

- Writes\_FlexRAM — minimum number of writes to each FlexRAM location
- EEPROM — allocated FlexNVM based on DEPART; entered with Program Partition command
- EESIZE — allocated FlexRAM based on DEPART; entered with Program Partition command
- Write\_efficiency —
  - 0.25 for 8-bit writes to FlexRAM
  - 0.50 for 16-bit or 32-bit writes to FlexRAM
- $n_{\text{nvmcycd}}$  — data flash cycling endurance

**Figure 7. EEPROM backup writes to FlexRAM**

## 6.4.2 EzPort Switching Specifications

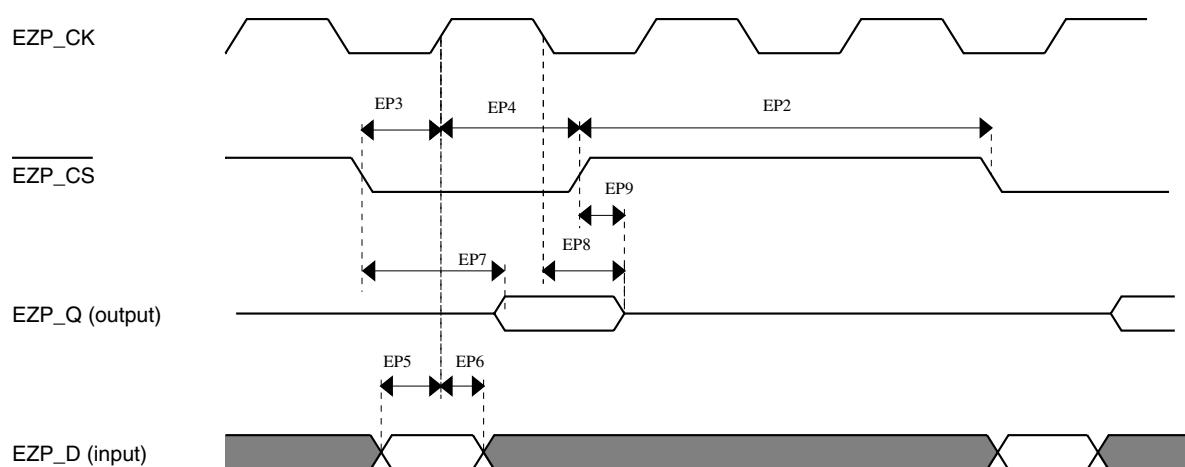
**Table 23. EzPort switching specifications**

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V

*Table continues on the next page...*

**Table 23. EzPort switching specifications (continued)**

Num	Description	Min.	Max.	Unit
EP1	EZP_CK frequency of operation (all commands except READ)	—	$f_{SYS}/2$	MHz
EP1a	EZP_CK frequency of operation (READ command)	—	$f_{SYS}/8$	MHz
EP2	EZP_CS negation to next EZP_CS assertion	$2 \times t_{EZP\_CK}$	—	ns
EP3	EZP_CS input valid to EZP_CK high (setup)	5	—	ns
EP4	EZP_CK high to EZP_CS input invalid (hold)	5	—	ns
EP5	EZP_D input valid to EZP_CK high (setup)	2	—	ns
EP6	EZP_CK high to EZP_D input invalid (hold)	5	—	ns
EP7	EZP_CK low to EZP_Q output valid	—	17	ns
EP8	EZP_CK low to EZP_Q output invalid (hold)	0	—	ns
EP9	EZP_CS negation to EZP_Q tri-state	—	12	ns

**Figure 8. EzPort Timing Diagram**

## 6.5 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

## 6.6 Analog

## 6.6.1 ADC electrical specifications

The 16-bit accuracy specifications listed in [Table 24](#) and [Table 25](#) are achievable on the differential pins ADC<sub>x</sub>\_DP0, ADC<sub>x</sub>\_DM0.

All other ADC channels meet the 13-bit differential/12-bit single-ended accuracy specifications.

### 6.6.1.1 16-bit ADC operating conditions

**Table 24. 16-bit ADC operating conditions**

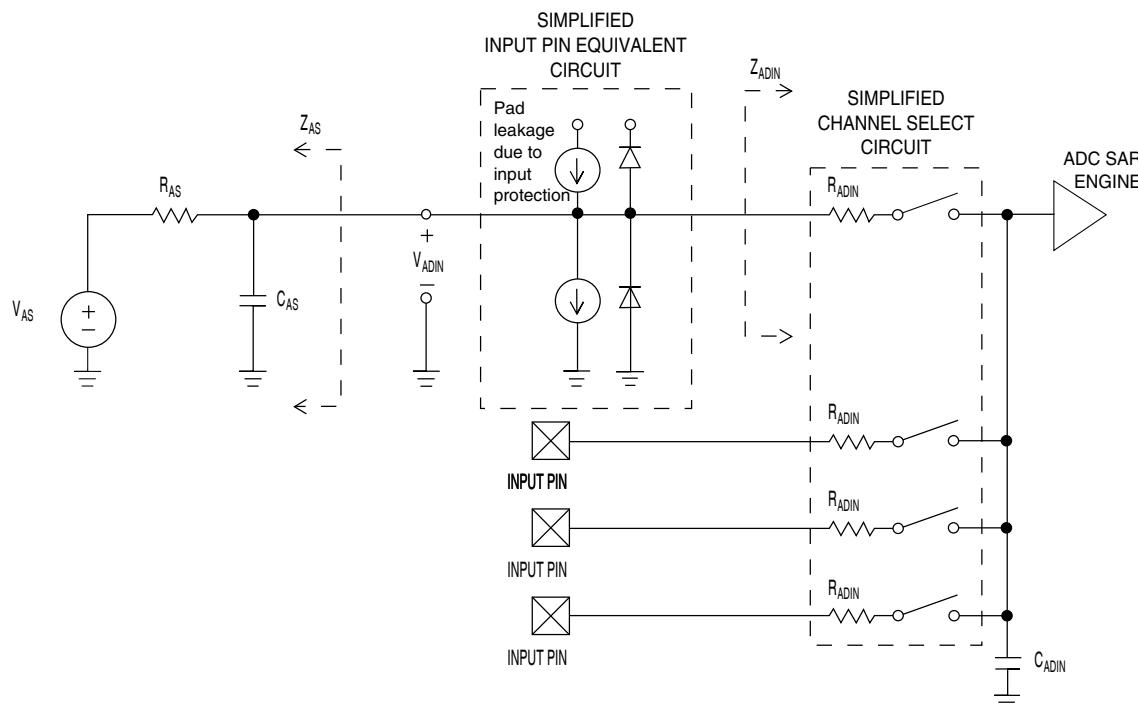
Symbol	Description	Conditions	Min.	Typ. <sup>1</sup>	Max.	Unit	Notes
V <sub>DDA</sub>	Supply voltage	Absolute	1.71	—	3.6	V	
ΔV <sub>DDA</sub>	Supply voltage	Delta to V <sub>DD</sub> (V <sub>DD</sub> -V <sub>DDA</sub> )	-100	0	+100	mV	<a href="#">2</a>
ΔV <sub>SSA</sub>	Ground voltage	Delta to V <sub>SS</sub> (V <sub>SS</sub> -V <sub>SSA</sub> )	-100	0	+100	mV	<a href="#">2</a>
V <sub>REFH</sub>	ADC reference voltage high		1.13	V <sub>DDA</sub>	V <sub>DDA</sub>	V	
V <sub>REFL</sub>	Reference voltage low		V <sub>SSA</sub>	V <sub>SSA</sub>	V <sub>SSA</sub>	V	
V <sub>ADIN</sub>	Input voltage		V <sub>REFL</sub>	—	V <sub>REFH</sub>	V	
C <sub>ADIN</sub>	Input capacitance	<ul style="list-style-type: none"> <li>• 16 bit modes</li> <li>• 8/10/12 bit modes</li> </ul>	— —	8 4	10 5	pF	
R <sub>ADIN</sub>	Input resistance		—	2	5	kΩ	
R <sub>AS</sub>	Analog source resistance	13/12 bit modes f <sub>ADCK</sub> < 4MHz	—	—	5	kΩ	<a href="#">3</a>
f <sub>ADCK</sub>	ADC conversion clock frequency	≤ 13 bit modes	1.0	—	18.0	MHz	<a href="#">4</a>
f <sub>ADCK</sub>	ADC conversion clock frequency	16 bit modes	2.0	—	12.0	MHz	<a href="#">4</a>
C <sub>rate</sub>	ADC conversion rate	≤ 13 bit modes No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	20.000	—	818.330	Ksps	<a href="#">5</a>

Table continues on the next page...

**Table 24. 16-bit ADC operating conditions (continued)**

Symbol	Description	Conditions	Min.	Typ. <sup>1</sup>	Max.	Unit	Notes
C <sub>rate</sub>	ADC conversion rate	16 bit modes No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	37.037	—	461.467	Ksps	5

1. Typical values assume V<sub>DDA</sub> = 3.0 V, Temp = 25°C, f<sub>ADCK</sub> = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2. DC potential difference.
3. This resistance is external to MCU. The analog source resistance should be kept as low as possible in order to achieve the best results. The results in this datasheet were derived from a system which has <8 Ω analog source resistance. The R<sub>AS</sub>/C<sub>AS</sub> time constant should be kept to <1ns.
4. To use the maximum ADC conversion clock frequency, the ADHSC bit should be set and the ADLPC bit should be clear.
5. For guidelines and examples of conversion rate calculation, download the ADC calculator tool: [http://cache.freescale.com/files/soft\\_dev\\_tools/software/app\\_software/converters/ADC\\_CALCULATOR\\_CNV.zip?fpst=1](http://cache.freescale.com/files/soft_dev_tools/software/app_software/converters/ADC_CALCULATOR_CNV.zip?fpst=1)

**Figure 9. ADC input impedance equivalency diagram**

### 6.6.1.2 16-bit ADC electrical characteristics

**Table 25. 16-bit ADC characteristics (V<sub>REFH</sub> = V<sub>DDA</sub>, V<sub>REFL</sub> = V<sub>SSA</sub>)**

Symbol	Description	Conditions <sup>1</sup>	Min.	Typ. <sup>2</sup>	Max.	Unit	Notes
I <sub>DDA_ADC</sub>	Supply current		0.215	—	1.7	mA	3

*Table continues on the next page...*

**Table 25. 16-bit ADC characteristics ( $V_{REFH} = V_{DDA}$ ,  $V_{REFL} = V_{SSA}$ ) (continued)**

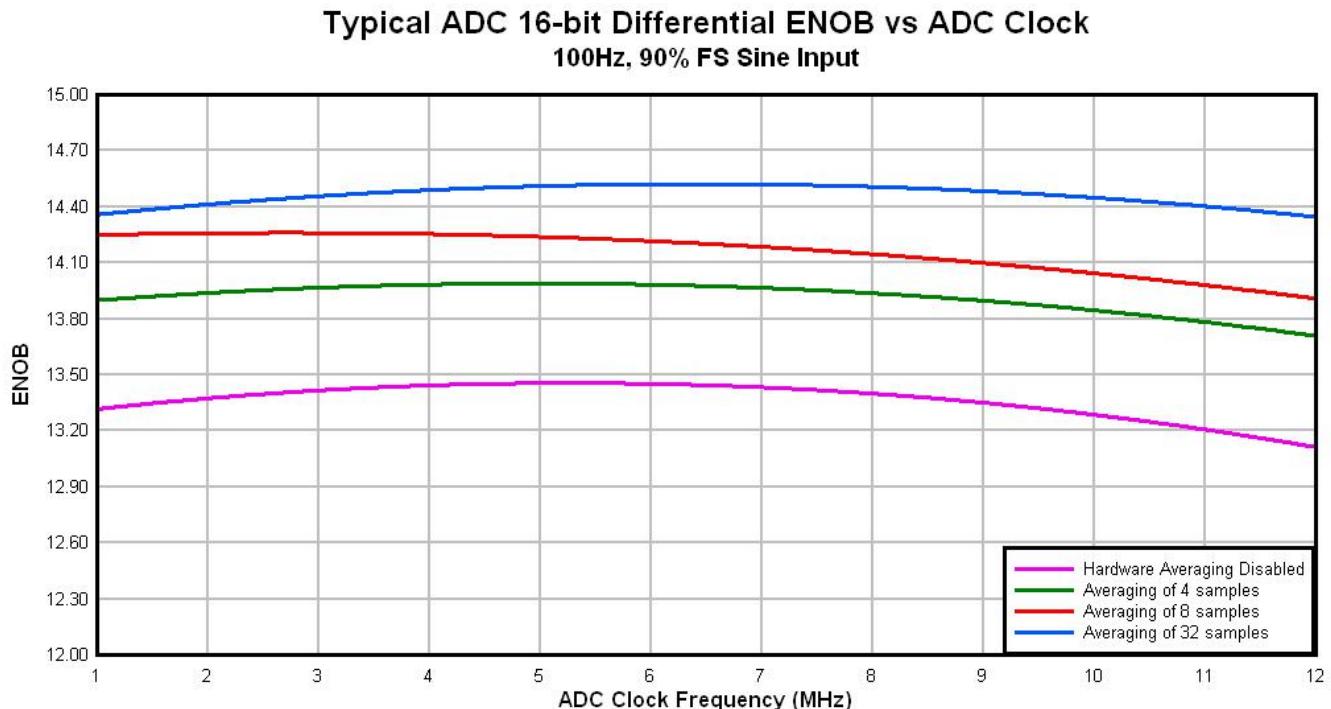
Symbol	Description	Conditions <sup>1</sup>	Min.	Typ. <sup>2</sup>	Max.	Unit	Notes
$f_{ADACK}$	ADC asynchronous clock source	<ul style="list-style-type: none"> <li>• ADLPC=1, ADHSC=0</li> <li>• ADLPC=1, ADHSC=1</li> <li>• ADLPC=0, ADHSC=0</li> <li>• ADLPC=0, ADHSC=1</li> </ul>	1.2 3.0 2.4 4.4	2.4 4.0 5.2 6.2	3.9 7.3 6.1 9.5	MHz MHz MHz MHz	$t_{ADACK} = 1/f_{ADACK}$
	Sample Time	See Reference Manual chapter for sample times					
TUE	Total unadjusted error	<ul style="list-style-type: none"> <li>• 12 bit modes</li> <li>• &lt;12 bit modes</li> </ul>	— —	$\pm 4$ $\pm 1.4$	$\pm 6.8$ $\pm 2.1$	LSB <sup>4</sup>	5
DNL	Differential non-linearity	<ul style="list-style-type: none"> <li>• 12 bit modes</li> <li>• &lt;12 bit modes</li> </ul>	— —	$\pm 0.7$ $\pm 0.2$	-1.1 to +1.9 -0.3 to 0.5	LSB <sup>4</sup>	5
INL	Integral non-linearity	<ul style="list-style-type: none"> <li>• 12 bit modes</li> <li>• &lt;12 bit modes</li> </ul>	— —	$\pm 1.0$ $\pm 0.5$	-2.7 to +1.9 -0.7 to +0.5	LSB <sup>4</sup>	5
$E_{FS}$	Full-scale error	<ul style="list-style-type: none"> <li>• 12 bit modes</li> <li>• &lt;12 bit modes</li> </ul>	— —	-4 -1.4	-5.4 -1.8	LSB <sup>4</sup>	$V_{ADIN} = V_{DDA}$ 5
$E_Q$	Quantization error	<ul style="list-style-type: none"> <li>• 16 bit modes</li> <li>• ≤13 bit modes</li> </ul>	— —	-1 to 0 —	— $\pm 0.5$	LSB <sup>4</sup>	
ENOB	Effective number of bits	16 bit differential mode <ul style="list-style-type: none"> <li>• Avg=32</li> <li>• Avg=4</li> </ul> 16 bit single-ended mode <ul style="list-style-type: none"> <li>• Avg=32</li> <li>• Avg=4</li> </ul>	12.8 11.9 12.2 11.4	14.5 13.8 13.9 13.1	— — — —	bits bits bits bits	6
SINAD	Signal-to-noise plus distortion	See ENOB	$6.02 \times ENOB + 1.76$			dB	
THD	Total harmonic distortion	16 bit differential mode <ul style="list-style-type: none"> <li>• Avg=32</li> </ul> 16 bit single-ended mode <ul style="list-style-type: none"> <li>• Avg=32</li> </ul>	— —	-94 -85	— —	dB dB	7

Table continues on the next page...

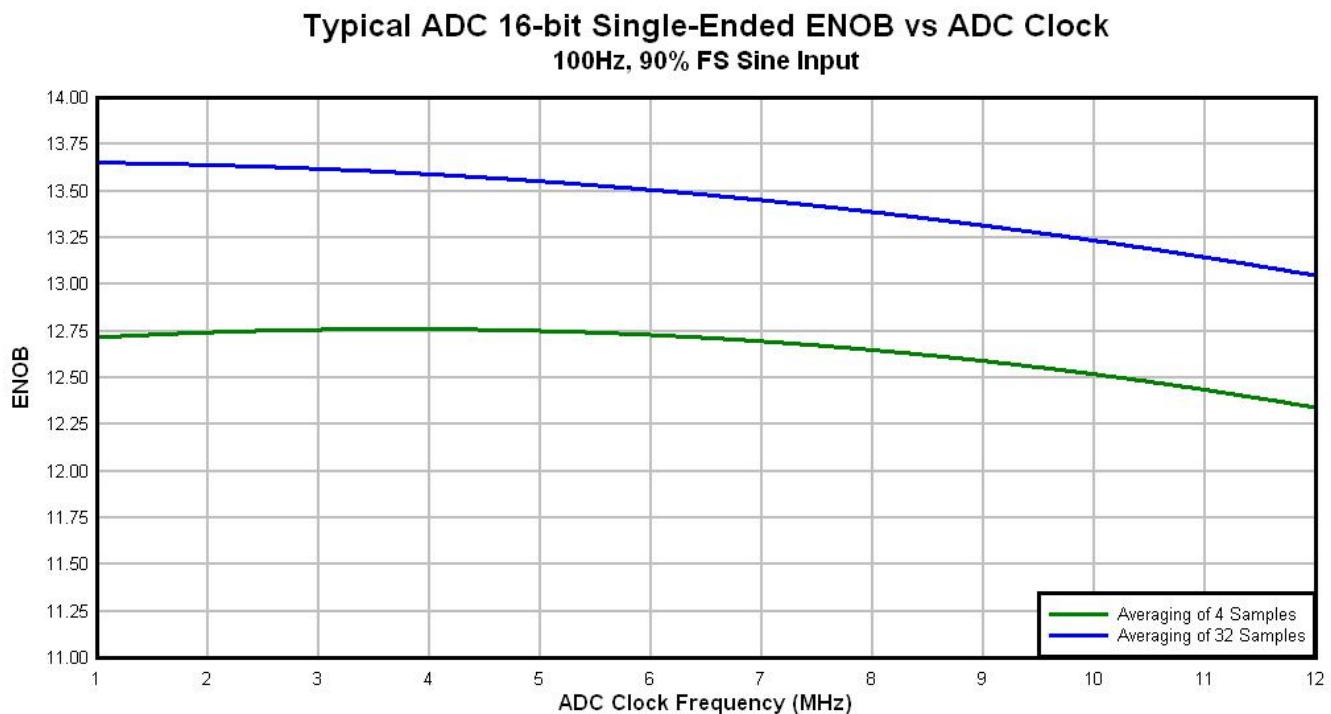
**Table 25. 16-bit ADC characteristics ( $V_{REFH} = V_{DDA}$ ,  $V_{REFL} = V_{SSA}$ ) (continued)**

Symbol	Description	Conditions <sup>1</sup>	Min.	Typ. <sup>2</sup>	Max.	Unit	Notes
SFDR	Spurious free dynamic range	16 bit differential mode • Avg=32	82	95	—	dB	<sup>7</sup>
		16 bit single-ended mode • Avg=32	78	90	—	dB	
E <sub>IL</sub>	Input leakage error	$I_{in} \times R_{AS}$				mV	$I_{in}$ = leakage current (refer to the MCU's voltage and current operating ratings)
	Temp sensor slope	−40°C to 105°C		—	1.715	—	mV/°C
V <sub>TEMP25</sub>	Temp sensor voltage	25°C		—	719	—	mV

1. All accuracy numbers assume the ADC is calibrated with  $V_{REFH} = V_{DDA}$
2. Typical values assume  $V_{DDA} = 3.0$  V, Temp = 25°C,  $f_{ADCK} = 2.0$  MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
3. The ADC supply current depends on the ADC conversion clock speed, conversion rate and the ADLPC bit (low power). For lowest power operation the ADLPC bit should be set, the HSC bit should be clear with 1MHz ADC conversion clock speed.
4. 1 LSB =  $(V_{REFH} - V_{REFL})/2^N$
5. ADC conversion clock <16MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
6. Input data is 100 Hz sine wave. ADC conversion clock <12MHz.
7. Input data is 1 kHz sine wave. ADC conversion clock <12MHz.



**Figure 10. Typical ENOB vs. ADC\_CLK for 16-bit differential mode**



**Figure 11. Typical ENOB vs. ADC\_CLK for 16-bit single-ended mode**

## 6.6.2 CMP and 6-bit DAC electrical specifications

**Table 26. Comparator and 6-bit DAC electrical specifications**

Symbol	Description	Min.	Typ.	Max.	Unit
$V_{DD}$	Supply voltage	1.71	—	3.6	V
$I_{DDHS}$	Supply current, High-speed mode (EN=1, PMODE=1)	—	—	200	$\mu A$
$I_{DDLS}$	Supply current, low-speed mode (EN=1, PMODE=0)	—	—	20	$\mu A$
$V_{AIN}$	Analog input voltage	$V_{SS} - 0.3$	—	$V_{DD}$	V
$V_{AIO}$	Analog input offset voltage	—	—	20	mV
$V_H$	Analog comparator hysteresis <sup>1</sup>				
	• CR0[HYSTCTR] = 00	—	5	—	mV
	• CR0[HYSTCTR] = 01	—	10	—	mV
	• CR0[HYSTCTR] = 10	—	20	—	mV
	• CR0[HYSTCTR] = 11	—	30	—	mV
$V_{CMPOH}$	Output high	$V_{DD} - 0.5$	—	—	V
$V_{CMPOI}$	Output low	—	—	0.5	V
$t_{DHS}$	Propagation delay, high-speed mode (EN=1, PMODE=1)	20	50	200	ns
$t_{DLS}$	Propagation delay, low-speed mode (EN=1, PMODE=0)	80	250	600	ns
	Analog comparator initialization delay <sup>2</sup>	—	—	40	$\mu s$
$I_{DAC6b}$	6-bit DAC current adder (enabled)	—	7	—	$\mu A$
INL	6-bit DAC integral non-linearity	-0.5	—	0.5	LSB <sup>3</sup>
DNL	6-bit DAC differential non-linearity	-0.3	—	0.3	LSB

1. Typical hysteresis is measured with input voltage range limited to 0.6 to  $V_{DD}-0.6V$ .
2. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to DACEN, VRSEL, PSEL, MSEL, VOSEL) and the comparator output settling to a stable level.
3. 1 LSB =  $V_{reference}/64$

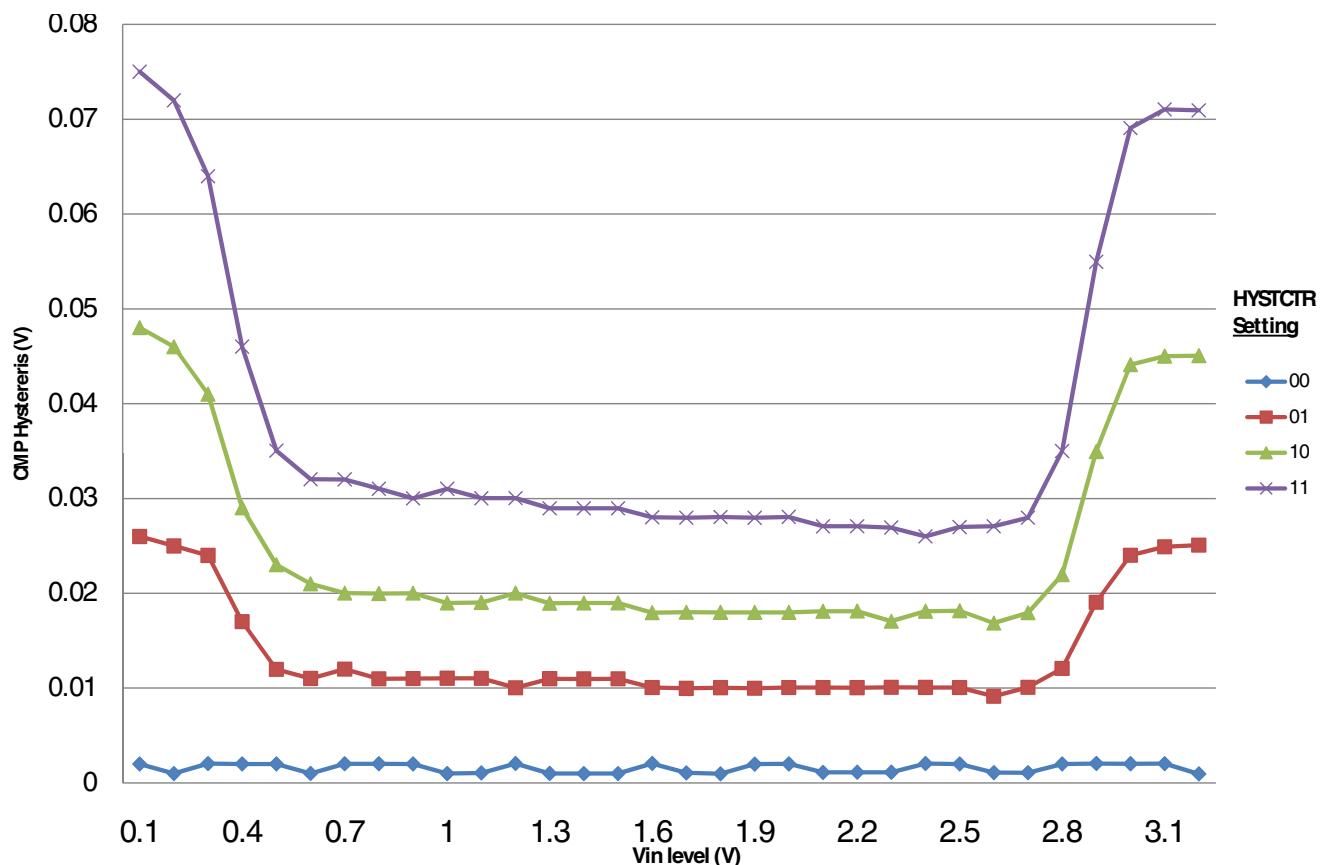


Figure 12. Typical hysteresis vs. Vin level (VDD=3.3V, PMODE=0)

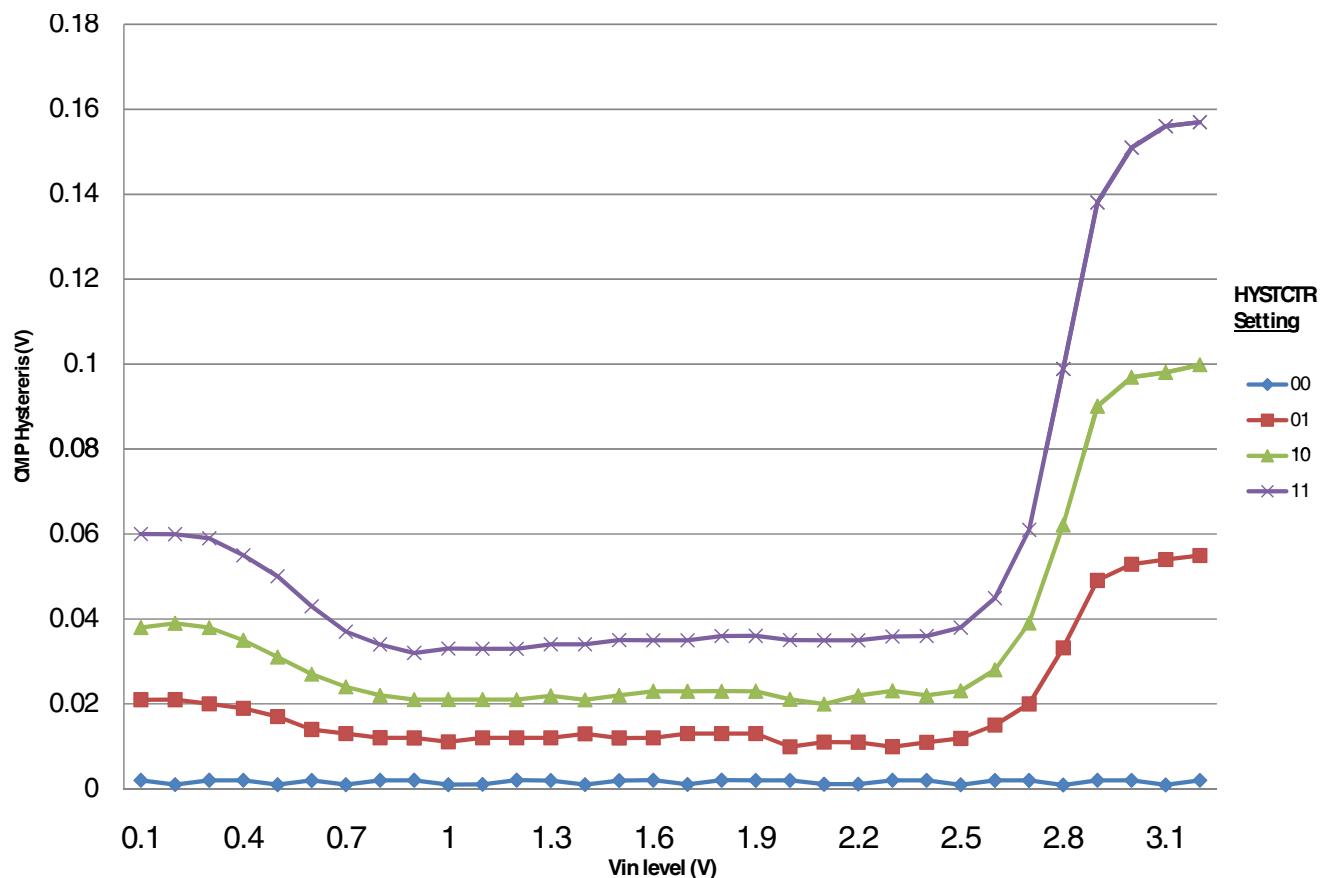


Figure 13. Typical hysteresis vs. Vin level (VDD=3.3V, PMODE=1)

### 6.6.3 Voltage reference electrical specifications

Table 27. VREF full-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V <sub>DDA</sub>	Supply voltage	1.71	3.6	V	
T <sub>A</sub>	Temperature	-40	105	°C	
C <sub>L</sub>	Output load capacitance	100		nF	1

1. C<sub>L</sub> must be connected to VREF\_OUT if the VREF\_OUT functionality is being used for either an internal or external reference.

Table 28. VREF full-range operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V <sub>out</sub>	Voltage reference output with factory trim at nominal V <sub>DDA</sub> and temperature=25C	1.1965	1.2	1.2027	V	
V <sub>out</sub>	Voltage reference output with— factory trim	1.1584	—	1.2376	V	

Table continues on the next page...

**Table 28. VREF full-range operating behaviors (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$V_{out}$	Voltage reference output — user trim	1.198	—	1.202	V	
$V_{step}$	Voltage reference trim step	—	0.5	—	mV	
$V_{tdrift}$	Temperature drift ( $V_{max} - V_{min}$ across the full temperature range)	—	—	80	mV	
Ac	Aging coefficient	—	—	400	uV/yr	
$I_{bg}$	Bandgap only (MODE_LV = 00) current	—	—	80	μA	
$I_{tr}$	Low power buffer (MODE_LV = 10) current	—	—	1.1	mA	
$\Delta V_{LOAD}$	Load regulation (MODE_LV = 10)				mV	1
	• current = + 1.0 mA	—	2	—		
	• current = - 1.0 mA	—	5	—		
$T_{stup}$	Buffer startup time	—	—	100	μs	
$V_{vdrift}$	Voltage drift ( $V_{max} - V_{min}$ across the full voltage range) (MODE_LV = 10, REGEN = 1)	—	2	—	mV	

1. Load regulation voltage is the difference between the VREF\_OUT voltage with no load vs. voltage with defined load

**Table 29. VREF limited-range operating requirements**

Symbol	Description	Min.	Max.	Unit	Notes
$T_A$	Temperature	0	50	°C	

**Table 30. VREF limited-range operating behaviors**

Symbol	Description	Min.	Max.	Unit	Notes
$V_{out}$	Voltage reference output with factory trim	1.173	1.225	V	

## 6.7 Timers

See [General switching specifications](#).

## 6.8 Communication interfaces

## 6.8.1 USB electrical specifications

The USB electicals for the USB On-the-Go module conform to the standards documented by the Universal Serial Bus Implementers Forum. For the most up-to-date standards, visit <http://www.usb.org>.

## 6.8.2 USB DCD electrical specifications

**Table 31. USB DCD electrical specifications**

Symbol	Description	Min.	Typ.	Max.	Unit
$V_{DP\_SRC}$	USB_DP source voltage (up to 250 $\mu$ A)	0.5	—	0.7	V
$V_{LGC}$	Threshold voltage for logic high	0.8	—	2.0	V
$I_{DP\_SRC}$	USB_DP source current	7	10	13	$\mu$ A
$I_{DM\_SINK}$	USB_DM sink current	50	100	150	$\mu$ A
$R_{DM\_DWN}$	D-pulldown resistance for data pin contact detect	14.25	—	24.8	k $\Omega$
$V_{DAT\_REF}$	Data detect voltage	0.25	0.33	0.4	V

## 6.8.3 USB VREG electrical specifications

**Table 32. USB VREG electrical specifications**

Symbol	Description	Min.	Typ. <sup>1</sup>	Max.	Unit	Notes
$V_{REGIN}$	Input supply voltage	2.7	—	5.5	V	
$I_{DDon}$	Quiescent current — Run mode, load current equal zero, input supply ( $V_{REGIN}$ ) > 3.6 V	—	120	186	$\mu$ A	
$I_{DDstby}$	Quiescent current — Standby mode, load current equal zero	—	1.1	1.54	$\mu$ A	
$I_{DDoff}$	Quiescent current — Shutdown mode <ul style="list-style-type: none"> <li>• <math>V_{REGIN} = 5.0</math> V and temperature=25C</li> <li>• Across operating voltage and temperature</li> </ul>	—	650	—	nA	
$I_{LOADrun}$	Maximum load current — Run mode	—	—	120	mA	
$I_{LOADstby}$	Maximum load current — Standby mode	—	—	1	mA	
$V_{Reg33out}$	Regulator output voltage — Input supply ( $V_{REGIN}$ ) > 3.6 V <ul style="list-style-type: none"> <li>• Run mode</li> <li>• Standby mode</li> </ul>	3 2.1	3.3 2.8	3.6 3.6	V V	
$V_{Reg33out}$	Regulator output voltage — Input supply ( $V_{REGIN}$ ) < 3.6 V, pass-through mode	2.1	—	3.6	V	<sup>2</sup>

Table continues on the next page...

**Table 32. USB VREG electrical specifications  
(continued)**

Symbol	Description	Min.	Typ. <sup>1</sup>	Max.	Unit	Notes
C <sub>OUT</sub>	External output capacitor	1.76	2.2	8.16	μF	
ESR	External output capacitor equivalent series resistance	1	—	100	mΩ	
I <sub>LIM</sub>	Short circuit current	—	290	—	mA	

1. Typical values assume VREGIN = 5.0 V, Temp = 25 °C unless otherwise stated.  
 2. Operating in pass-through mode: regulator output voltage equal to the input voltage minus a drop proportional to I<sub>Load</sub>.

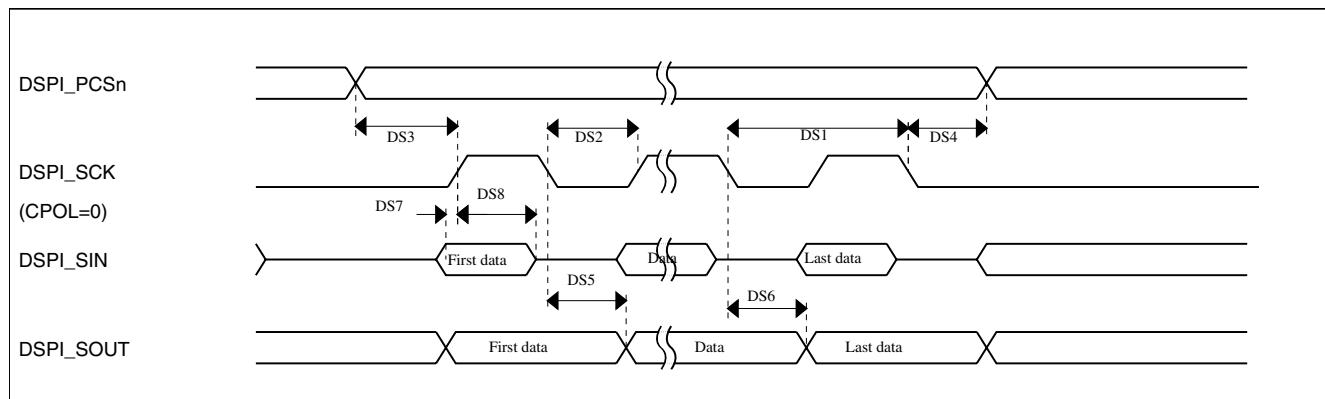
## 6.8.4 DSPI switching specifications (limited voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provide DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

**Table 33. Master mode DSPI timing (limited voltage range)**

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	2.7	3.6	V	
	Frequency of operation	—	25	MHz	
DS1	DSPI_SCK output cycle time	2 × t <sub>BUS</sub>	—	ns	
DS2	DSPI_SCK output high/low time	(t <sub>SCK</sub> /2) – 2	(t <sub>SCK</sub> /2) + 2	ns	
DS3	DSPI_PCS <sub>n</sub> valid to DSPI_SCK delay	(t <sub>BUS</sub> × 2) – 2	—	ns	<sup>1</sup>
DS4	DSPI_SCK to DSPI_PCS <sub>n</sub> invalid delay	(t <sub>BUS</sub> × 2) – 2	—	ns	<sup>2</sup>
DS5	DSPI_SCK to DSPI_SOUT valid	—	8.5	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	–2	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	15	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

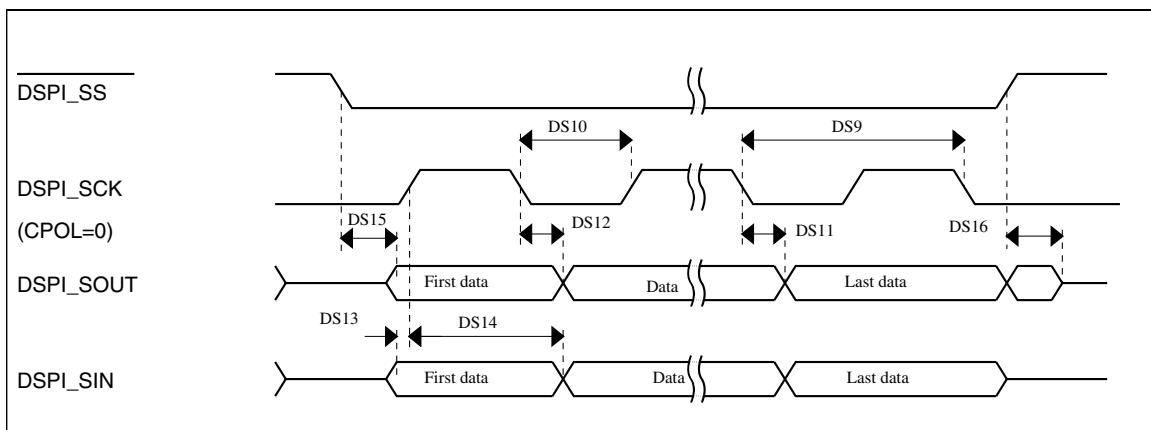
1. The delay is programmable in SPIx\_CTARn[PSSCK] and SPIx\_CTARn[CSSCK].  
 2. The delay is programmable in SPIx\_CTARn[PASC] and SPIx\_CTARn[ASC].



**Figure 14. DSPI classic SPI timing — master mode**

**Table 34. Slave mode DSPI timing (limited voltage range)**

Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
	Frequency of operation		12.5	MHz
DS9	DSPI_SCK input cycle time	$4 \times t_{BUS}$	—	ns
DS10	DSPI_SCK input high/low time	$(t_{SCK}/2) - 2$	$(t_{SCK}/2) + 2$	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	10	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	DSPI_SS active to DSPI_SOUT driven	—	14	ns
DS16	DSPI_SS inactive to DSPI_SOUT not driven	—	14	ns



**Figure 15. DSPI classic SPI timing — slave mode**

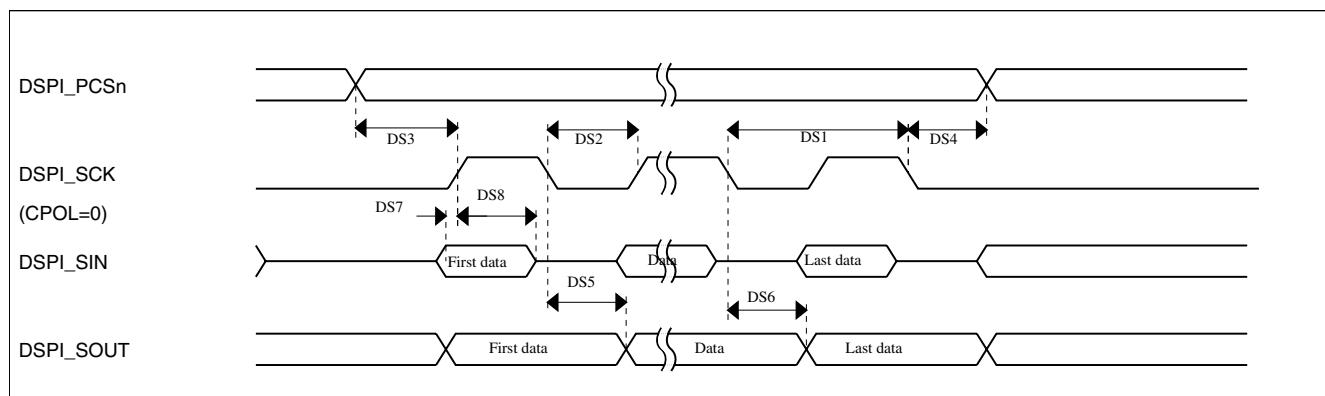
## 6.8.5 DSPI switching specifications (full voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provides DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

**Table 35. Master mode DSPI timing (full voltage range)**

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	1.71	3.6	V	<a href="#">1</a>
	Frequency of operation	—	12.5	MHz	
DS1	DSPI_SCK output cycle time	$4 \times t_{BUS}$	—	ns	
DS2	DSPI_SCK output high/low time	$(t_{SCK}/2) - 4$	$(t_{SCK}/2) + 4$	ns	
DS3	DSPI_PCSn valid to DSPI_SCK delay	$(t_{BUS} \times 2) - 4$	—	ns	<a href="#">2</a>
DS4	DSPI_SCK to DSPI_PCSn invalid delay	$(t_{BUS} \times 2) - 4$	—	ns	<a href="#">3</a>
DS5	DSPI_SCK to DSPI_SOUT valid	—	10	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	-4.5	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	20.5	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

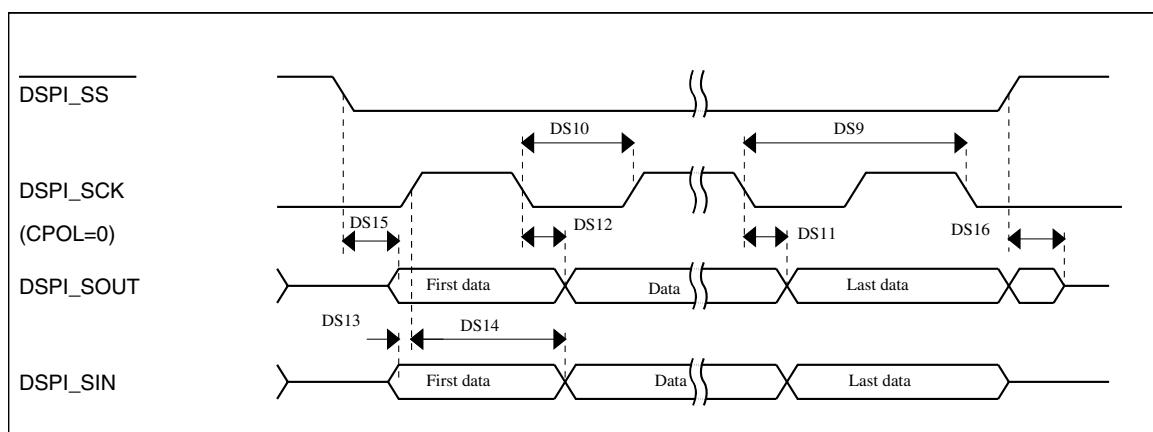
1. The DSPI module can operate across the entire operating voltage for the processor, but to run across the full voltage range the maximum frequency of operation is reduced.
2. The delay is programmable in SPIx\_CTARn[PSSCK] and SPIx\_CTARn[CSSCK].
3. The delay is programmable in SPIx\_CTARn[PASC] and SPIx\_CTARn[ASC].



**Figure 16. DSPI classic SPI timing — master mode**

**Table 36. Slave mode DSPI timing (full voltage range)**

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
	Frequency of operation	—	6.25	MHz
DS9	DSPI_SCK input cycle time	$8 \times t_{BUS}$	—	ns
DS10	DSPI_SCK input high/low time	$(t_{SCK}/2) - 4$	$(t_{SCK}/2) + 4$	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	20	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	DSPI_SS active to DSPI_SOUT driven	—	19	ns
DS16	DSPI_SS inactive to DSPI_SOUT not driven	—	19	ns

**Figure 17. DSPI classic SPI timing — slave mode**

### 6.8.6 I<sup>2</sup>C switching specifications

See [General switching specifications](#).

### 6.8.7 UART switching specifications

See [General switching specifications](#).

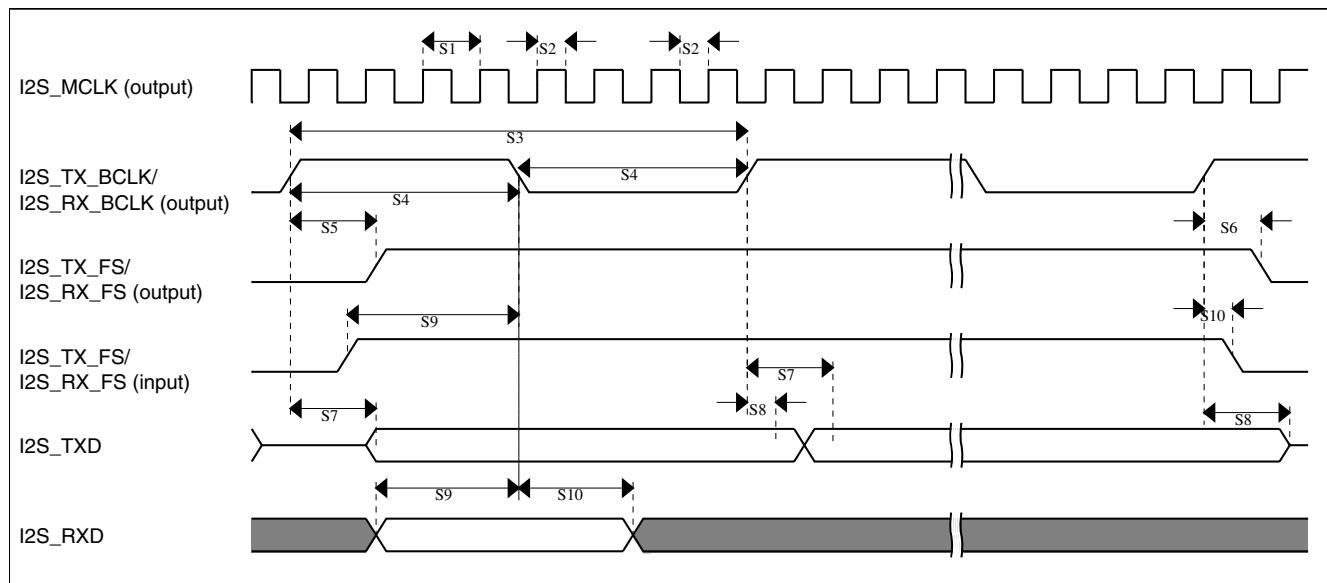
## 6.8.8 I2S/SAI Switching Specifications

This section provides the AC timing for the I2S/SAI module in master mode (clocks are driven) and slave mode (clocks are input). All timing is given for noninverted serial clock polarity (TCR2[BCP] is 0, RCR2[BCP] is 0) and a noninverted frame sync (TCR4[FSP] is 0, RCR4[FSP] is 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the bit clock signal (BCLK) and/or the frame sync (FS) signal shown in the following figures.

**Table 37. I2S/SAI master mode timing**

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time <sup>1</sup>	40		ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK cycle time (output) <sup>1</sup>	80	—	ns
	I2S_RX_BCLK cycle time (output) <sup>1</sup>	160	—	
S4	I2S_TX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	—	15	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	0	—	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	15	ns
S8	I2S_TX_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	25	—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns
S11	I2S_TX_FS input assertion to I2S_TXD output valid <sup>2</sup>	—	21	ns

1. This parameter is limited in VLPx modes.
2. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

**Figure 18. I2S/SAI timing — master modes****Table 38. I2S/SAI slave mode timing**

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_RX_BCLK cycle time (input)	80	—	ns
	I2S_TX_BCLK cycle time (input)	160	—	
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	10	—	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	2	—	ns
S15	I2S_TX_BCLK to I2S_TxD/I2S_TX_FS output valid	—	29	ns
S16	I2S_TX_BCLK to I2S_TxD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	10	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	2	—	ns
S19	I2S_TX_FS input assertion to I2S_TxD output valid <sup>1</sup>	—	21	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

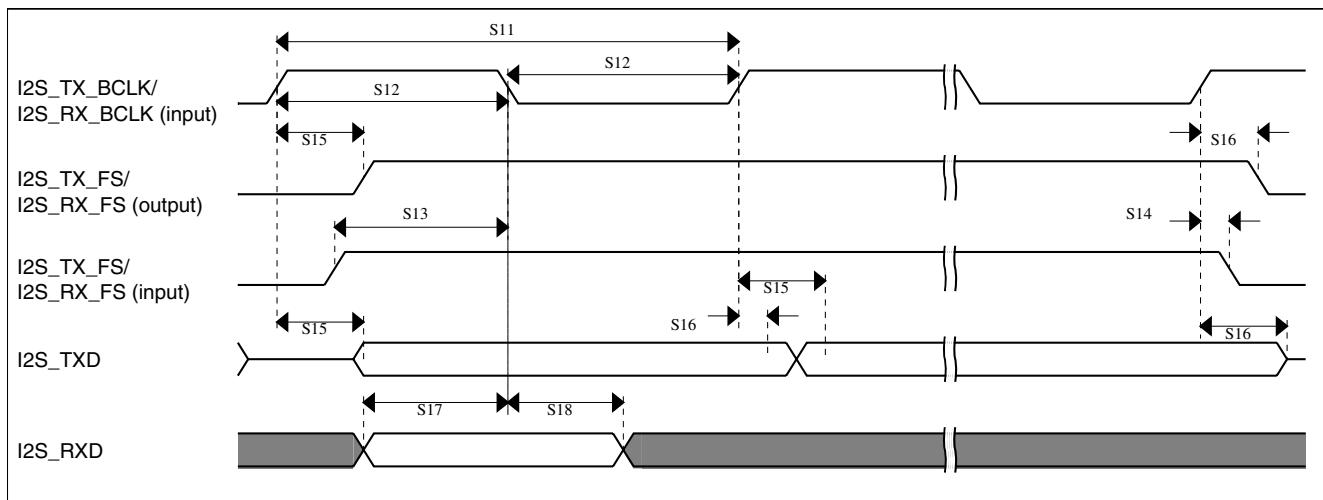


Figure 19. I2S/SAI timing — slave modes

## 6.9 Human-machine interfaces (HMI)

### 6.9.1 TSI electrical specifications

Table 39. TSI electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$V_{DDTSI}$	Operating voltage	1.71	—	3.6	V	
$C_{ELE}$	Target electrode capacitance range	1	20	500	pF	1
$f_{REFmax}$	Reference oscillator frequency	—	8	TBD	MHz	2
$f_{ELEmax}$	Electrode oscillator frequency	—	0.5	TBD	MHz	2
$C_{REF}$	Internal reference capacitor	TBD	1	TBD	pF	
$V_{\Delta}$	Oscillator delta voltage	TBD	600	TBD	mV	2
$I_{REF}$	Reference oscillator current source base current • 1uA setting (REFCHRG=0) • 32uA setting (REFCHRG=31)	—	1.133	1.5	$\mu$ A	2, 3
$I_{ELE}$	Electrode oscillator current source base current • 1uA setting (EXTCHRG=0) • 32uA setting (EXTCHRG=31)	—	1.133	1.5	$\mu$ A	2, 4
Pres5	Electrode capacitance measurement precision	—	8.3333	38400	%	5
Pres20	Electrode capacitance measurement precision	—	8.3333	38400	%	6
Pres100	Electrode capacitance measurement precision	—	8.3333	38400	%	7
MaxSens	Maximum sensitivity	0.003	12.5	—	fF/count	8
Res	Resolution	—	—	16	bits	

Table continues on the next page...

**Table 39. TSI electrical specifications (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
T <sub>Con20</sub>	Response time @ 20 pF	8	15	25	μs	9
I <sub>TSI_RUN</sub>	Current added in run mode	—	55	—	μA	
I <sub>TSI_LP</sub>	Low power mode current adder	—	1.3	TBD	μA	10

1. The TSI module is functional with capacitance values outside this range. However, optimal performance is not guaranteed.
2. Fixed external capacitance of 20 pF.
3. The programmable current source value is generated by multiplying the SCANC[REFCHRG] value and the base current.
4. The programmable current source value is generated by multiplying the SCANC[EXTCHRG] value and the base current.
5. Measured with a 5 pF electrode, reference oscillator frequency of 10 MHz, PS = 128, NSCN = 8; I<sub>ext</sub> = 16.
6. Measured with a 20 pF electrode, reference oscillator frequency of 10 MHz, PS = 128, NSCN = 2; I<sub>ext</sub> = 16.
7. Measured with a 20 pF electrode, reference oscillator frequency of 10 MHz, PS = 16, NSCN = 3; I<sub>ext</sub> = 16.
8. Sensitivity defines the minimum capacitance change when a single count from the TSI module changes, it is equal to  $(C_{ref} * I_{ext}) / (I_{ref} * PS * NSCN)$ . Sensitivity depends on the configuration used. The typical value listed is based on the following configuration: I<sub>ext</sub> = 5 μA, EXTCHRG = 4, PS = 128, NSCN = 2, I<sub>ref</sub> = 16 μA, REFCHRG = 15, C<sub>ref</sub> = 1.0 pF. The minimum sensitivity describes the smallest possible capacitance that can be measured by a single count (this is the best sensitivity but is described as a minimum because it's the smallest number). The minimum sensitivity parameter is based on the following configuration: I<sub>ext</sub> = 1 μA, EXTCHRG = 0, PS = 128, NSCN = 32, I<sub>ref</sub> = 32 μA, REFCHRG = 31, C<sub>ref</sub> = 0.5 pF
9. Time to do one complete measurement of the electrode. Sensitivity resolution of 0.0133 pF, PS = 0, NSCN = 0, 1 electrode, EXTCHRG = 15.
10. REFCHRG=0, EXTCHRG=4, PS=7, NSCN=0F, LPSCNITV=F, LPO is selected (1 kHz), and fixed external capacitance of 20 pF. Data is captured with an average of 7 periods window.

## 7 Dimensions

### 7.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to <http://www.freescale.com> and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
48-pin LQFP	98ASH00962A
48-pin QFN	98ARH99048A

## 8 Pinout

## 8.1 K10 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

48 LQF P- QFN	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
1	VDD	VDD	VDD								
2	VSS	VSS	VSS								
3	PTE16	ADC0_SE4a	ADC0_SE4a	PTE16	SPI0_PCS0	UART2_TX	FTM_CLKIN0		FTM0_FLT3		
4	PTE17	ADC0_SE5a	ADC0_SE5a	PTE17	SPI0_SCK	UART2_RX	FTM_CLKIN1		LPTMR0_ALT3		
5	PTE18	ADC0_SE6a	ADC0_SE6a	PTE18	SPI0_SOUT	UART2_CTS_b	I2C0_SDA				
6	PTE19	ADC0_SE7a	ADC0_SE7a	PTE19	SPI0_SIN	UART2_RTS_b	I2C0_SCL				
7	ADC0_DP0	ADC0_DP0	ADC0_DP0								
8	ADC0_DM0	ADC0_DM0	ADC0_DM0								
9	VDDA	VDDA	VDDA								
10	VREFH	VREFH	VREFH								
11	VREFL	VREFL	VREFL								
12	VSSA	VSSA	VSSA								
13	VREF_OUT/ CMP1_IN5/ CMP0_IN5	VREF_OUT/ CMP1_IN5/ CMP0_IN5	VREF_OUT/ CMP1_IN5/ CMP0_IN5								
14	XTAL32	XTAL32	XTAL32								
15	EXTAL32	EXTAL32	EXTAL32								
16	VBAT	VBAT	VBAT								
17	PTA0	JTAG_TCLK/ SWD_CLK/ EZP_CLK	TSI0_CH1	PTA0	UART0_CTS_b/ UART0_COL_b	FTM0_CH5			JTAG_TCLK/ SWD_CLK	EZP_CLK	
18	PTA1	JTAG_TDI/ EZP_DI	TSI0_CH2	PTA1	UART0_RX	FTM0_CH6			JTAG_TDI	EZP_DI	
19	PTA2	JTAG_TDO/ TRACE_SW O/EZP_DO	TSI0_CH3	PTA2	UART0_TX	FTM0_CH7			JTAG_TDO/ TRACE_SW O	EZP_DO	
20	PTA3	JTAG_TMS/ SWD_DIO	TSI0_CH4	PTA3	UART0_RTS_b	FTM0_CH0			JTAG_TMS/ SWD_DIO		
21	PTA4/ LLWU_P3	NMI_b/ EZP_CS_b	TSI0_CH5	PTA4/ LLWU_P3		FTM0_CH1			NMI_b	EZP_CS_b	
22	VDD	VDD	VDD								
23	VSS	VSS	VSS								
24	PTA18	EXTAL0	EXTAL0	PTA18		FTM0_FLT2	FTM_CLKIN0				

## Pinout

48 LQF P- QFN	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
25	PTA19	XTAL0	XTAL0	PTA19		FTM1_FLT0	FTM_CLKIN1		LPTMR0_ALT1		
26	RESET_b	RESET_b	RESET_b								
27	PTB0/ LLWU_P5	ADC0_SE8/ TSI0_CH0	ADC0_SE8/ TSI0_CH0	PTB0/ LLWU_P5	I2C0_SCL	FTM1_CH0			FTM1_QD_PA		
28	PTB1	ADC0_SE9/ TSI0_CH6	ADC0_SE9/ TSI0_CH6	PTB1	I2C0_SDA	FTM1_CH1			FTM1_QD_PHB		
29	PTB2	ADC0_SE12/ TSI0_CH7	ADC0_SE12/ TSI0_CH7	PTB2	I2C0_SCL	UART0_RTS_b			FTM0_FLT3		
30	PTB3	ADC0_SE13/ TSI0_CH8	ADC0_SE13/ TSI0_CH8	PTB3	I2C0_SDA	UART0_CTS_b/ UART0_COL_b			FTM0_FLT0		
31	PTB16	TSI0_CH9	TSI0_CH9	PTB16		UART0_RX			EWM_IN		
32	PTB17	TSI0_CH10	TSI0_CH10	PTB17		UART0_TX			EWM_OUT_b		
33	PTC0	ADC0_SE14/ TSI0_CH13	ADC0_SE14/ TSI0_CH13	PTC0	SPI0_PCS4	PDB0_EXTRG					
34	PTC1/ LLWU_P6	ADC0_SE15/ TSI0_CH14	ADC0_SE15/ TSI0_CH14	PTC1/ LLWU_P6	SPI0_PCS3	UART1_RTS_b	FTM0_CH0		I2S0_TXD0		
35	PTC2	ADC0_SE4b/ CMP1_IN0/ TSI0_CH15	ADC0_SE4b/ CMP1_IN0/ TSI0_CH15	PTC2	SPI0_PCS2	UART1_CTS_b	FTM0_CH1		I2S0_TX_FS		
36	PTC3/ LLWU_P7	CMP1_IN1	CMP1_IN1	PTC3/ LLWU_P7	SPI0_PCS1	UART1_RX	FTM0_CH2		I2S0_TX_BCLK		
37	PTC4/ LLWU_P8	DISABLED		PTC4/ LLWU_P8	SPI0_PCS0	UART1_TX	FTM0_CH3		CMP1_OUT		
38	PTC5/ LLWU_P9	DISABLED		PTC5/ LLWU_P9	SPI0_SCK	LPTMR0_ALT2	I2S0_RXD0		CMP0_OUT		
39	PTC6/ LLWU_P10	CMP0_IN0	CMP0_IN0	PTC6/ LLWU_P10	SPI0_SOUT	PDB0_EXTRG	I2S0_RX_BCLK		I2S0_MCLK		
40	PTC7	CMP0_IN1	CMP0_IN1	PTC7	SPI0_SIN		I2S0_RX_FS				
41	PTD0/ LLWU_P12	DISABLED		PTD0/ LLWU_P12	SPI0_PCS0	UART2_RTS_b					
42	PTD1	ADC0_SE5b	ADC0_SE5b	PTD1	SPI0_SCK	UART2_CTS_b					
43	PTD2/ LLWU_P13	DISABLED		PTD2/ LLWU_P13	SPI0_SOUT	UART2_RX					
44	PTD3	DISABLED		PTD3	SPI0_SIN	UART2_TX					
45	PTD4/ LLWU_P14	DISABLED		PTD4/ LLWU_P14	SPI0_PCS1	UART0_RTS_b	FTM0_CH4		EWM_IN		
46	PTD5	ADC0_SE6b	ADC0_SE6b	PTD5	SPI0_PCS2	UART0_CTS_b/ UART0_COL_b	FTM0_CH5		EWM_OUT_b		
47	PTD6/ LLWU_P15	ADC0_SE7b	ADC0_SE7b	PTD6/ LLWU_P15	SPI0_PCS3	UART0_RX	FTM0_CH6		FTM0_FLT0		

48 LQF P- QFN	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
48	PTD7	DISABLED		PTD7	CMT_IRO	UART0_TX	FTM0_CH7		FTM0_FLT1		

## 8.2 K10 Pinouts

The below figure shows the pinout diagram for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see the previous section.

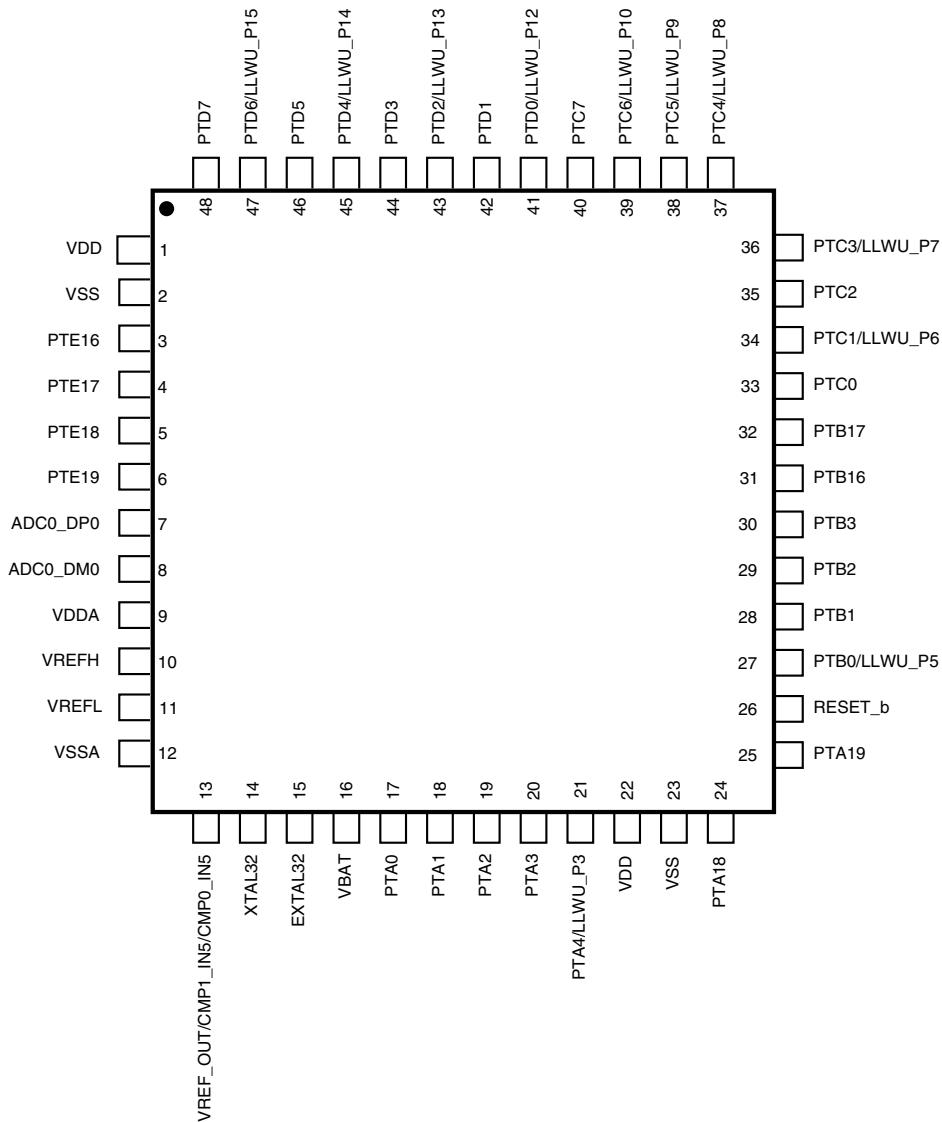


Figure 20. K10 48 LQFP/QFN Pinout Diagram

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