EFM32®

... the world's most energy friendly microcontrollers

TINY GECKO DATASHEET

EFM32TG110F32/EFM32TG110F16/EFM32TG110F8/EFM32TG110F4

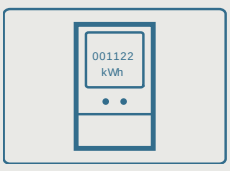
0 1 2 3 4

Preliminary

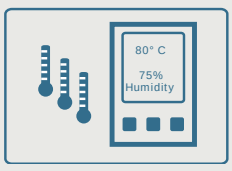
- **ARM Cortex-M3 CPU platform**
  - High Performance 32-bit processor @ up to 32 MHz
  - Wake-up Interrupt Controller
- **Flexible Energy Management System**
  - 20 nA @ 3 V Shutoff Mode
  - 0.6 µA @ 3 V Stop Mode, including Power-on Reset, Brown-out Detector, RAM and CPU retention
  - 0.9 µA @ 3 V Deep Sleep Mode, including Real Time Clock with 32.768 kHz oscillator, Power-on Reset, Brown-out Detector, RAM and CPU retention
  - 45 µA/MHz @ 3 V Sleep Mode
  - 180 µA/MHz @ 3 V Run Mode, with code executed from flash
- **32/16/8/4 KB Flash**
- **4/4/2/1 KB RAM**
- **17 General Purpose I/O pins**
  - Configurable Push-pull, Open-drain, pull-up/down, input filter, drive strength
  - Configurable peripheral I/O locations
  - 11 asynchronous external interrupts
- **8 Channel DMA Controller**
- **8 Channel Peripheral Reflex System for autonomous inter-peripheral signaling**
- **Hardware AES with 128/256-bit keys in 54/75 cycles**
- **Timers/Counters**
  - 2× 16-bit Timer/Counter
    - 2×3 Compare/Capture/PWM channels
  - 16-bit Low Energy Timer
  - 24-bit Real-Time Counter
  - 8-bit Pulse Counter
    - Asynchronous pulse counting/quadrature decoding
  - Watchdog Timer with dedicated RC oscillator @ 50 nA
- **Communication interfaces**
  - 2× Universal Synchronous/Asynchronous Receiver/Transmitter
    - UART/SPI/SmartCard (ISO 7816)/IrDA
    - Triple buffered full/half-duplex operation
    - 4-16 data bits
  - Low Energy UART
    - Autonomous operation with DMA in Deep Sleep Mode
  - I^2C Interface with SMBus support
    - Address recognition in Stop Mode
- **Ultra low power precision analog peripherals**
  - 12-bit 1 Msamples/s Analog to Digital Converter
    - 2 single ended channels/1 differential channels
    - On-chip temperature sensor
    - Conversion tailgating for predictable latency
  - 12-bit 500 ksamples/s Digital to Analog Converter
  - 2× Analog Comparator
    - Programmable speed/current
    - Capacitive sensing with up to 4 inputs
  - Supply Voltage Comparator
- **Ultra efficient Power-on Reset and Brown-Out Detector**
- **2-pin Serial Wire Debug interface**
  - 1-pin Serial Wire Viewer
- **Temperature range -40 to 85 ºC**
- **Single power supply 1.8 to 3.8 V**
- **QFN24 package**

EFM32TG110 microcontrollers are suited for all battery operated applications

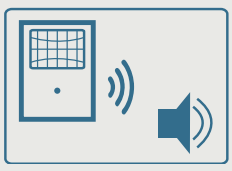
Energy Metering



Industrial/ Home Automation



Wireless Alarm/ Security



Medical Systems

ENERGY® micro

1 Ordering Information

Table 1.1 (p. 2) shows the available EFM32TG110 devices.

Table 1.1. Ordering Information

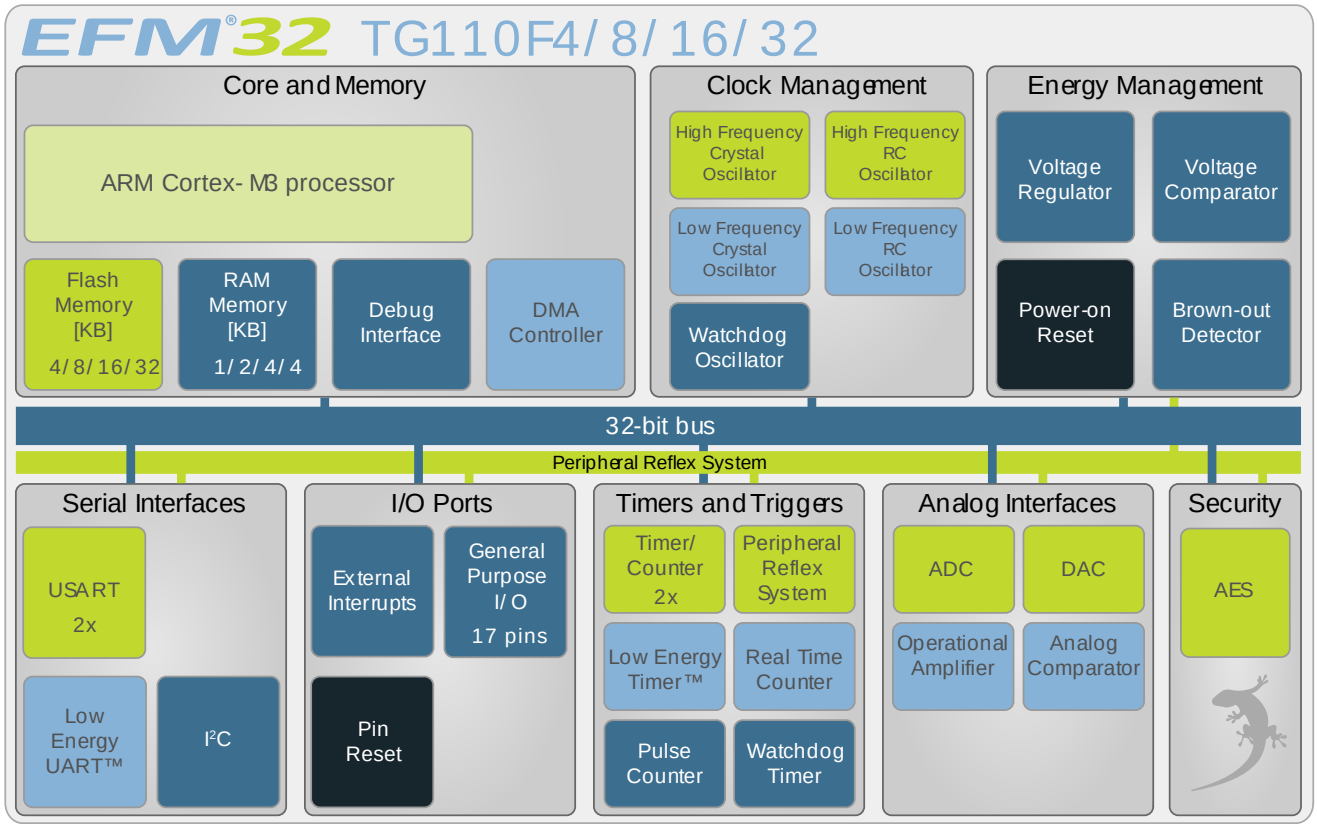
Ordering Code	Flash (KB)	RAM (KB)	Max Speed (MHz)	Supply Voltage	Temperature	Package
EFM32TG110F4-QFN24	4	1	32	1.8 to 3.8V	-40 to 85 ºC	QFN24
EFM32TG110F8-QFN24	8	2	32	1.8 to 3.8V	-40 to 85 ºC	QFN24
EFM32TG110F16-QFN24	16	4	32	1.8 to 3.8V	-40 to 85 ºC	QFN24
EFM32TG110F32-QFN24	32	4	32	1.8 to 3.8V	-40 to 85 ºC	QFN24

Visit **www.energymicro.com** for information on global distributors and representatives or contact **sales@energymicro.com** for additional information.

1.1 Block Diagram

A block diagram of the EFM32TG110 is shown in Figure 1.1 (p. 2) .

Figure 1.1. Block Diagram



2 System Summary

2.1 System Introduction

The EFM32G family of MCUs is the world's most energy friendly microcontroller. With a unique combination of the powerful 32-bit ARM Cortex-M3, innovative low energy techniques, short wake-up time from energy saving modes, and a wide selection of peripherals, the EFM32G microcontroller is well suited for any battery operated application as well as other systems requiring high performance and low-energy consumption. This section gives a short introduction to each of the modules in general terms and also and shows a summary of the configuration for the EFM32TG110 devices. For a complete feature set and in-depth information on the modules, the reader is referred to the *EFM32G Reference Manual*.

2.1.1 ARM Cortex-M3 Core

The ARM Cortex-M3 includes a 32-bit RISC processor which can achieve as much as 1.25 Dhrystone MIPS/MHz. A Memory Protection Unit with support for up to 8 memory segments is included, as well as a Wake-up Interrupt Controller handling interrupts triggered while the CPU is asleep. The EFM32 implementation of the Cortex-M3 is described in detail in *EFM32G Cortex-M3 Reference Manual*.

2.1.2 Debug Interface (DBG)

This device includes hardware debug support through a 2-pin serial-wire debug interface. In addition there is also a 1-wire Serial Wire Viewer pin which can be used to output profiling information, data trace and software-generated messages.

2.1.3 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the EFM32G microcontroller. The flash memory is readable and writable from both the Cortex-M3 and DMA. The flash memory is divided into two blocks; the main block and the information block. Program code is normally written to the main block. Additionally, the information block is available for special user data and flash lock bits. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in the energy modes EM0 and EM1.

2.1.4 Direct Memory Access Controller (DMA)

The Direct Memory Access (DMA) controller performs memory operations independently of the CPU. This has the benefit of reducing the energy consumption and the workload of the CPU, and enables the system to stay in low energy modes when moving for instance data from the USART to RAM or from the External Bus Interface to the DAC. The DMA controller uses the PL230 µDMA controller licensed from ARM.

2.1.5 Reset Management Unit (RMU)

The RMU is responsible for handling the reset functionality of the EFM32G.

2.1.6 Energy Management Unit (EMU)

The Energy Management Unit (EMU) manage all the low energy modes (EM) in EFM32G microcontrollers. Each energy mode manages if the CPU and the various peripherals are available. The EMU can also be used to turn off the power to unused SRAM blocks.

2.1.7 Clock Management Unit (CMU)

The Clock Management Unit (CMU) is responsible for controlling the oscillators and clocks on-board the EFM32G. The CMU provides the capability to turn on and off the clock on an individual basis to all

peripheral modules in addition to enable/disable and configure the available oscillators. The high degree of flexibility enables software to minimize energy consumption in any specific application by not wasting power on peripherals and oscillators that are inactive.

2.1.8 Watchdog (WDOG)

The purpose of the watchdog timer is to generate a reset in case of a system failure, to increase application reliability. The failure may e.g. be caused by an external event, such as an ESD pulse, or by a software failure.

2.1.9 Peripheral Reflex System (PRS)

The Peripheral Reflex System (PRS) system is a network which lets the different peripheral module communicate directly with each other without involving the CPU. Peripheral modules which send out Reflex signals are called producers. The PRS routes these reflex signals to consumer peripherals which apply actions depending on the data received. The format for the Reflex signals is not given, but edge triggers and other functionality can be applied by the PRS.

2.1.10 Inter-Integrated Circuit Interface (I2C)

The I^2C module provides an interface between the MCU and a serial I^2C-bus. It is capable of acting as both a master and a slave, and supports multi-master buses. Both standard-mode, fast-mode and fast-mode plus speeds are supported, allowing transmission rates all the way from 10 kbit/s up to 1 Mbit/s. Slave arbitration and timeouts are also provided to allow implementation of an SMBus compliant system. The interface provided to software by the I^2C module, allows both fine-grained control of the transmission process and close to automatic transfers. Automatic recognition of slave addresses is provided in all energy modes.

2.1.11 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The Universal Synchronous Asynchronous serial Receiver and Transmitter (USART) is a very flexible serial I/O module. It supports full duplex asynchronous UART communication as well as RS-485, SPI, MicroWire and 3-wire. It can also interface with ISO7816 SmartCards, and IrDA devices.

2.1.12 Low Energy Universal Asynchronous Receiver/Transmitter (LEUART)

The unique LEUART™, the Low Energy UART, is a UART that allows two-way UART communication on a strict power budget. Only a 32.768 kHz clock is needed to allow UART communication up to 9600 baud/s. The LEUART includes all necessary hardware support to make asynchronous serial communication possible with minimum of software intervention and energy consumption.

2.1.13 Timer/Counter (TIMER)

The 16-bit general purpose Timer has 3 compare/capture channels for input capture and compare/Pulse-Width Modulation (PWM) output.

2.1.14 Real Time Counter (RTC)

The Real Time Counter (RTC) contains a 24-bit counter and is clocked either by a 32.768 kHz crystal oscillator, or a 32 kHz RC oscillator. In addition to energy modes EM0 and EM1, the RTC is also available in EM2. This makes it ideal for keeping track of time since the RTC is enabled in EM2 where most of the device is powered down.

2.1.15 Low Energy Timer (LETIMER)

The unique LETIMER™, the Low Energy Timer, is a 16-bit timer that is available in energy mode EM2 in addition to EM1 and EM0. Because of this, it can be used for timing and output generation when most of the device is powered down, allowing simple tasks to be performed while the power consumption of the system is kept at an absolute minimum. The LETIMER can be used to output a variety of waveforms with minimal software intervention. It is also connected to the Real Time Counter (RTC), and can be configured to start counting on compare matches from the RTC.

2.1.16 Pulse Counter (PCNT)

The Pulse Counter (PCNT) can be used for counting pulses on a single input or to decode quadrature encoded inputs. It runs off either the internal LFACLK or the PCNTn_S0IN pin as external clock source. The module may operate in energy mode EM0 – EM3.

2.1.17 Analog Comparator (ACMP)

The Analog Comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs can either be one of the selectable internal references or from external pins. Response time and thereby also the current consumption can be configured by altering the current supply to the comparator.

2.1.18 Voltage Comparator (VCMP)

The Voltage Supply Comparator is used to monitor the supply voltage from software. An interrupt can be generated when the supply falls below or rises above a programmable threshold. Response time and thereby also the current consumption can be configured by altering the current supply to the comparator.

2.1.19 Analog to Digital Converter (ADC)

The ADC is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to one million samples per second. The integrated input mux can select inputs from >2 external pins and 6 internal signals.

2.1.20 Digital to Analog Converter (DAC)

The Digital to Analog Converter (DAC) can convert a digital value to an analog output voltage. The DAC is fully differential rail-to-rail, with 12-bit resolution. It has one single ended output buffer connected to channel 0. The DAC may be used for a number of different applications such as sensor interfaces or sound output.

2.1.21 Operational Amplifier (OPAMP)

The EFM32TG110 features 1 Operational Amplifier. The operational amplifier is a versatile general purpose amplifier with rail-to-rail differential input and rail-to-rail single ended output. The input can be set to pin, DAC or OPAMP, whereas the output can be pin, OPAMP or ADC. The current is programmable and the OPAMP has various internal configurations such as unity gain, programmable gain using internal resistors etc.

2.1.22 Advanced Encryption Standard Accelerator (AES)

The AES accelerator performs AES encryption and decryption with 128-bit or 256-bit keys. Encrypting or decrypting one 128-bit data block takes 52 HFCORECLK cycles with 128-bit keys and 75 HFCORECLK cycles with 256-bit keys. The AES module is an AHB slave which enables efficient access to the data and key registers. All write accesses to the AES module must be 32-bit operations, i.e. 8- or 16-bit operations are not supported.

2.1.23 General Purpose Input/Output (GPIO)

In the EFM32TG110, there are 17 General Purpose Input/Output (GPIO) pins, which are divided into ports with up to 16 pins each. These pins can individually be configured as either an output or input. More advances configurations like open-drain, filtering and drive strength can also be configured individually for the pins. The GPIO pins can also be overridden by peripheral pin connections, like Timer PWM outputs or USART communication, which can be routed to several locations on the device. The GPIO supports up to 16 asynchronous external pin interrupts, which enables interrupts from any pin on the device. Also, the input value of a pin can be routed through the Peripheral Reflex System to other peripherals.

2.2 Configuration Summary

The features of the EFM32TG110 is a subset of the feature set described in the EFM32G Reference Manual. Table 2.1 (p. 6) describes device specific implementation of the features.

Table 2.1. Configuration Summary

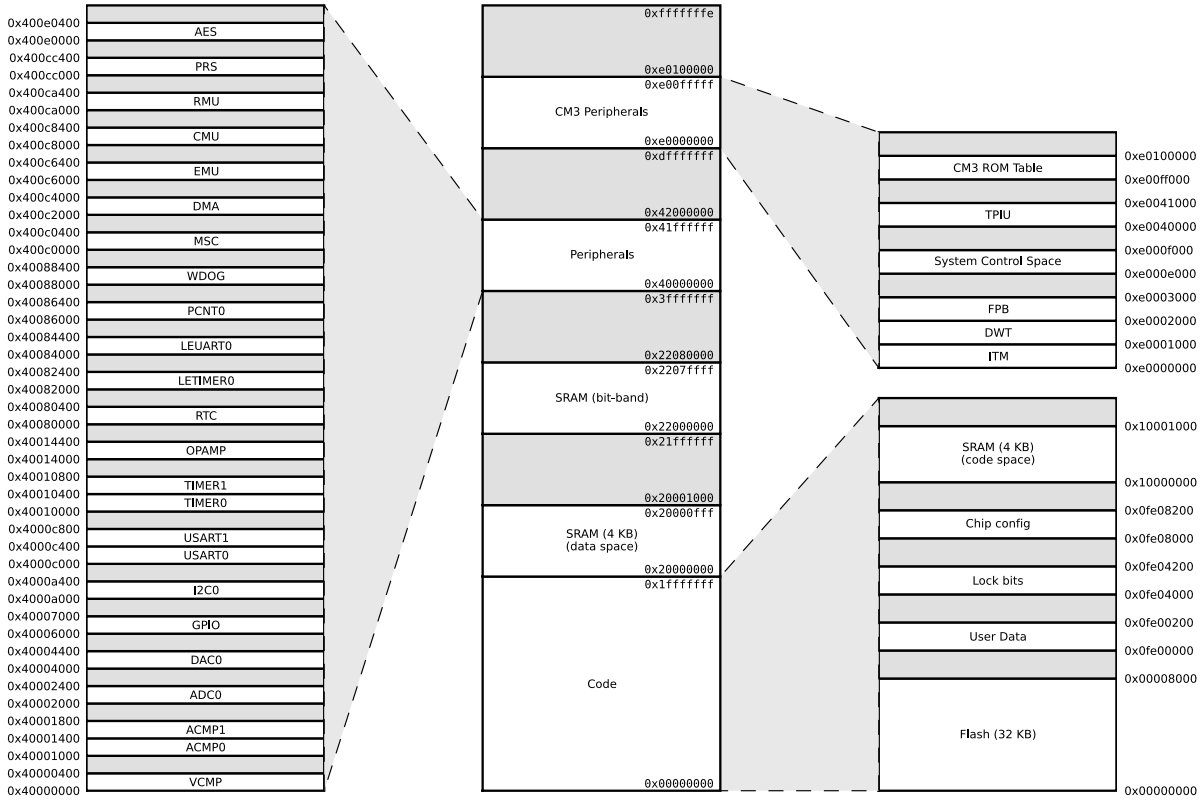
Module	Configuration	Pin Connections
Cortex-M3	Full configuration	NA
DBG	Full configuration	DBG_SWCLK, DBG_SWDIO, DBG_SWO
MSC	Full configuration	NA
DMA	Full configuration	NA
RMU	Full configuration	NA
EMU	Full configuration	NA
CMU	Full configuration	CMU_OUT0, CMU_OUT1
WDOG	Full configuration	NA
PRS	Full configuration	NA
I2C0	Full configuration	I2C0_SDA, I2C0_SCL
USART0	Full configuration	US0_TX, US0_RX. US0_CLK, US0_CS
USART1	No IrDA	US1_TX, US1_RX, US1_CLK, US1_CS
LEUART0	Full configuration	LEU0_TX, LEU0_RX
TIMER0	Full configuration	TIM0_CC[2:0]
TIMER1	Full configuration	TIM1_CC[2:0]
RTC	Full configuration	NA
LETIMER0	Full configuration	LET0_O[1:0]
PCNT0	16-bit count register	PCNT0_S[1:0]
ACMP0	Full configuration	ACMP0_CH[1:0], ACMP0_O
ACMP1	Full configuration	ACMP1_CH[1:0], ACMP1_O
VCMP	Full configuration	NA
ADC0	Full configuration	ADC0_CH[7:6]
DAC0	Full configuration	DAC0_OUT[0]
OPAMP	x1	Output: DAC0_OUT[0], Input: TBD.
AES	Full configuration	NA

Module	Configuration	Pin Connections
GPIO	17 pins	Available pins are shown in Table 4.3 (p. 40)

2.3 Memory Map

The *EFM32TG110* memory map is shown in Figure 2.1 (p. 7), with RAM and Flash sizes for the largest memory configuration.

Figure 2.1. EFM32TG110 Memory Map with largest RAM and Flash sizes



3 Electrical Characteristics

3.1 Test Conditions

3.1.1 Typical Values

The typical data are based on T_{AMB}=25°C and V_{DD}=3.0 V, as defined in Table 3.2 (p. 8), by simulation and/or technology characterisation unless otherwise specified.

3.1.2 Minimum and Maximum Values

The minimum and maximum values represent the worst conditions of ambient temperature, supply voltage and frequencies, as defined in Table 3.2 (p. 8), by simulation and/or technology characterisation unless otherwise specified.

3.2 Absolute Maximum Ratings

The absolute maximum ratings are stress ratings, and functional operation under such conditions are not guaranteed. Stress beyond the limits specified in Table 3.1 (p. 8) may affect the device reliability or cause permanent damage to the device. Functional operating conditions are given in Table 3.2 (p. 8) .

Table 3.1. Absolute Maximum Ratings

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{STG}	Storage temperature range		-40		85	°C
T_J	Maximum junction temperature	JEDEC J-STD-020D			260	°C
V_{DDMAX}	External main supply voltage		0		3.8	V
V_{IOPIN}	Voltage on any I/O pin		-0.3		V_{DD}+0.3	V

3.3 General Operating Conditions

3.3.1 General Operating Conditions

Table 3.2. General Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
T_{AMB}	Ambient temperature range	-40	25	85	°C
V_{DDOP}	Operating supply voltage	1.8	3.0	3.8	V
f_{APB}	Internal APB clock frequency			32	MHz
f_{AHB}	Internal AHB clock frequency			32	MHz

3.3.2 Environmental

Table 3.3. Environmental

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{ESDHBM}	ESD (Human Body Model HBM)	T_{AMB}=25°C			2	kV
V_{ESDCDM}	ESD (Charged Device Model, CDM)	T_{AMB}=25°C			500	V
MSL	Moisture sensitivity level	JEDEC J-STD-20D. Level 3			168	hrs
LU	Latchup sensitivity	JESD78 Latchup test procedure. Class II level A.			85	°C

3.4 Current Consumption

Table 3.4. Current Consumption

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{EM0}	EM0 current. No prescaling. Running prime number calculation code from Flash.	32 MHz HFXO, all peripheral clocks disabled, V_{DD}= 3.0 V		180		µA/MHz
		28 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V		181	235	µA/MHz
		21 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V		183	237	µA/MHz
		14 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V		185	243	µA/MHz
		11 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V		186	246	µA/MHz
		7 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V		191	257	µA/MHz
		1 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V		220		µA/MHz
I_{EM1}	EM1 current	32 MHz HFXO, all peripheral clocks disabled, V_{DD}= 3.0 V		45		µA/MHz
		28 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V		47	62	µA/MHz
		21 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V		48	64	µA/MHz
		14 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V		50	69	µA/MHz
		11 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V		51	72	µA/MHz
		7 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V		56	83	µA/MHz
		1 MHz HFRCO. all peripheral clocks disabled, V_{DD}= 3.0 V		103		µA/MHz
I_{EM2}	EM2 current	EM2 current with RTC at 1 Hz, RTC prescaled to 1kHz, 32 kHz LFRCO, V_{DD}= 3.0 V, T_{AMB}=25°C		0.9		µA
		EM2 current with RTC at 1 Hz, RTC prescaled to 1kHz, 32 kHz LFRCO, V_{DD}= 3.0 V, T_{AMB}=85°C		3.0	6.0	µA
I_{EM3}	EM3 current	V_{DD}= 3.0 V, T_{AMB}=25°C		0.59		µA
		V_{DD}= 3.0 V, T_{AMB}=85°C		2.75	5.8	µA
I_{EM4}	EM4 current	V_{DD}= 3.0 V, T_{AMB}=25°C		0.02		µA
		V_{DD}= 3.0 V, T_{AMB}=85°C		0.25	0.7	µA

Figure 3.1. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 28MHz

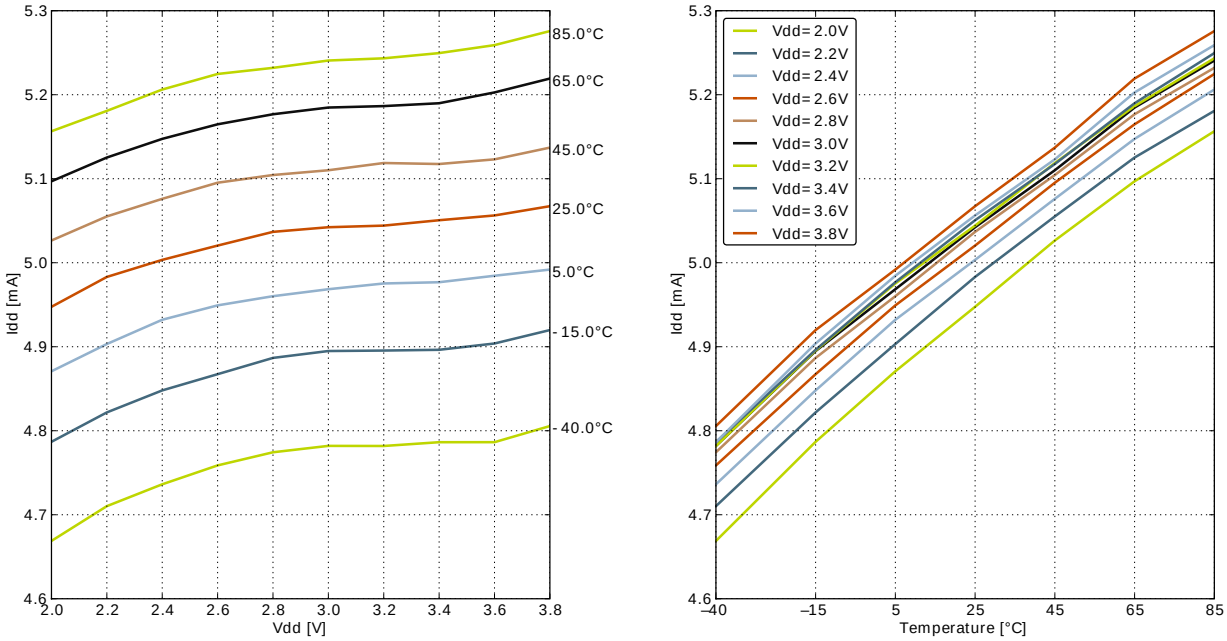


Figure 3.2. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 21MHz

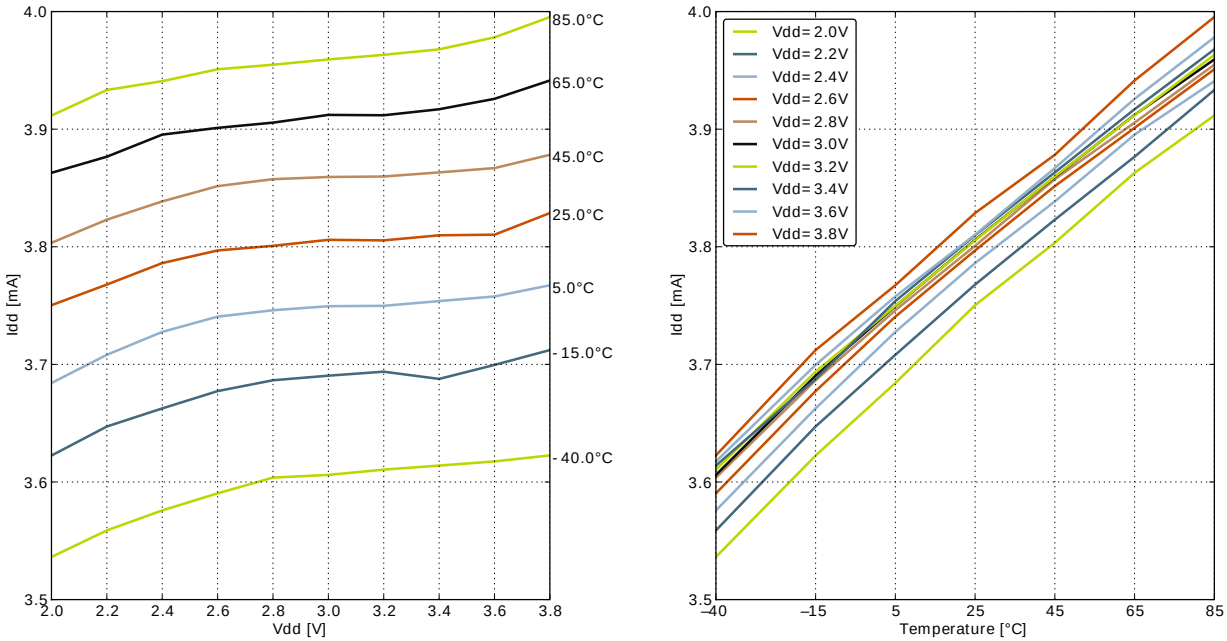


Figure 3.3. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 14MHz

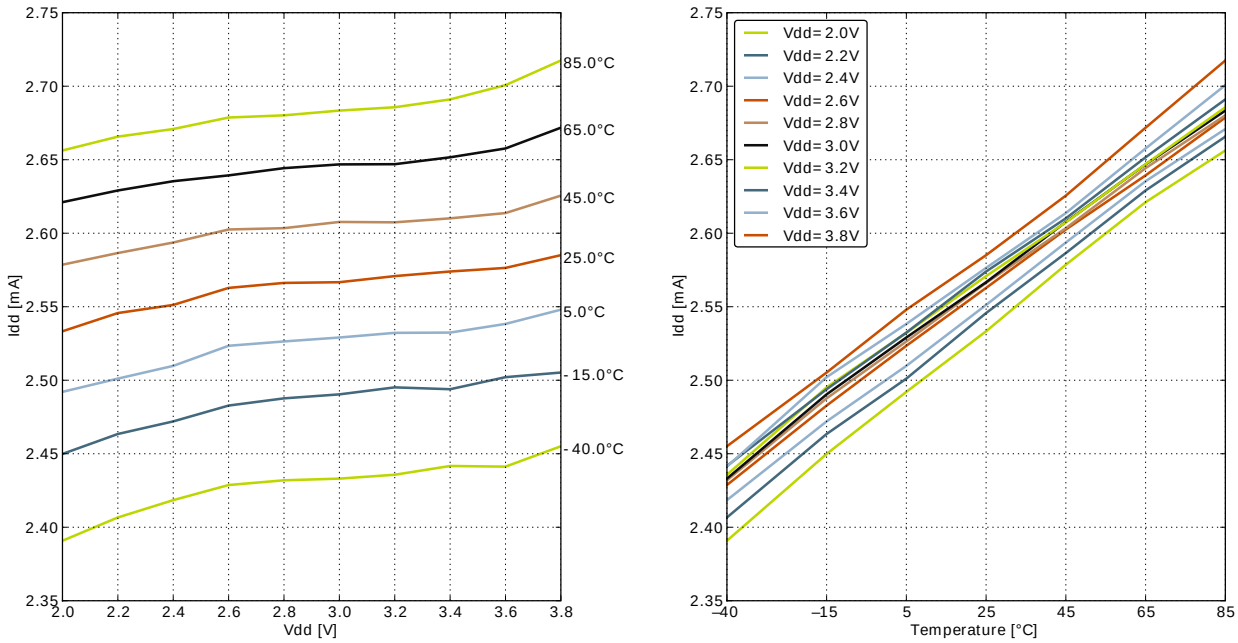


Figure 3.4. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 11MHz

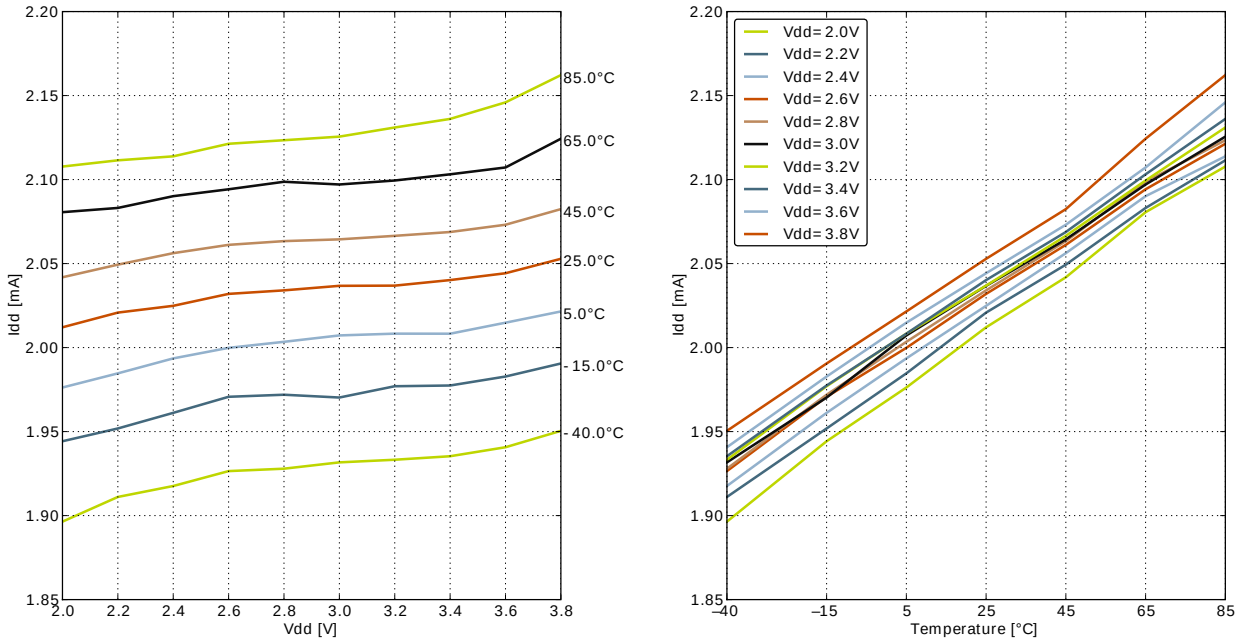


Figure 3.5. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 7MHz

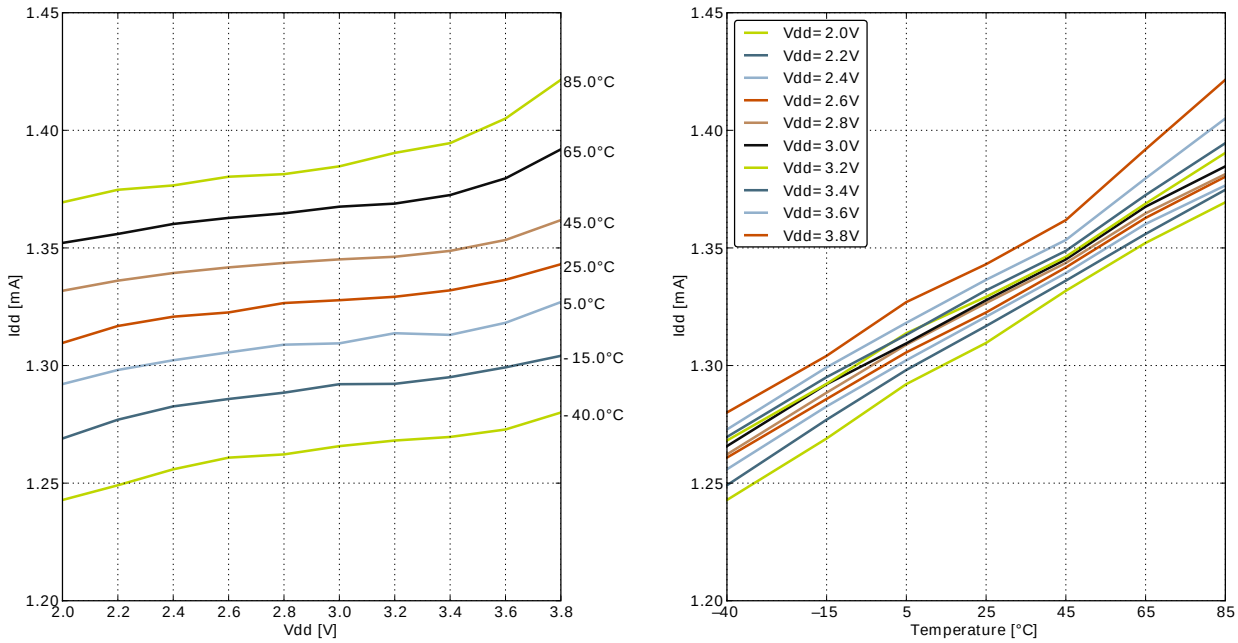


Figure 3.6. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 28MHz

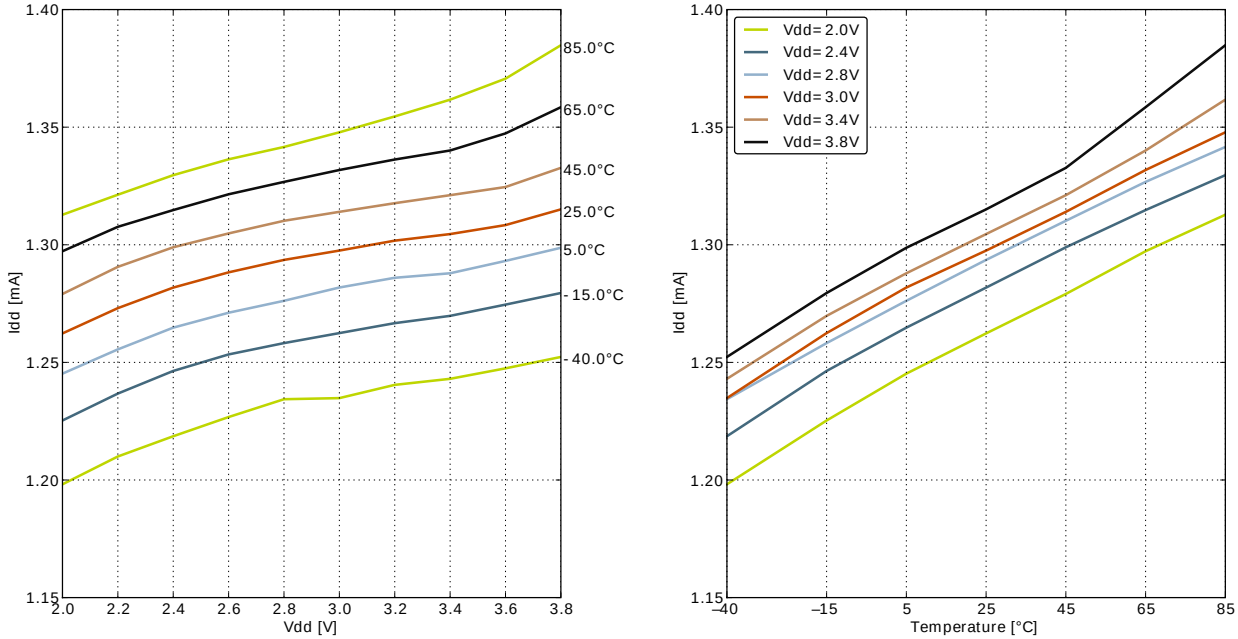


Figure 3.7. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 21MHz

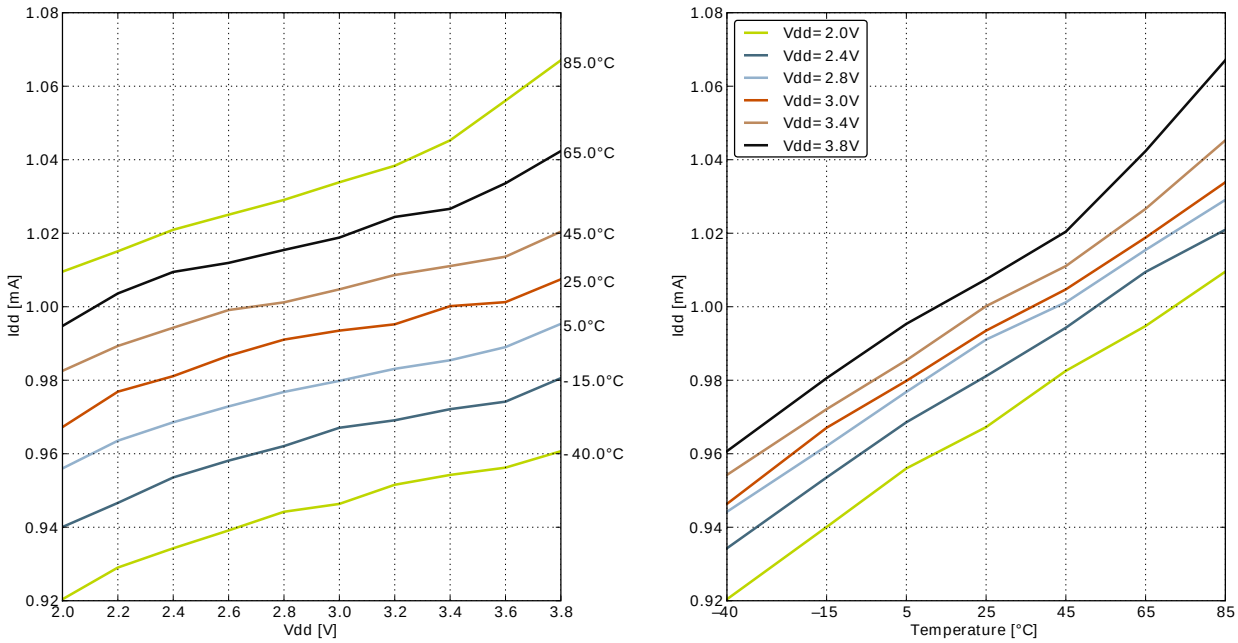


Figure 3.8. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 14MHz

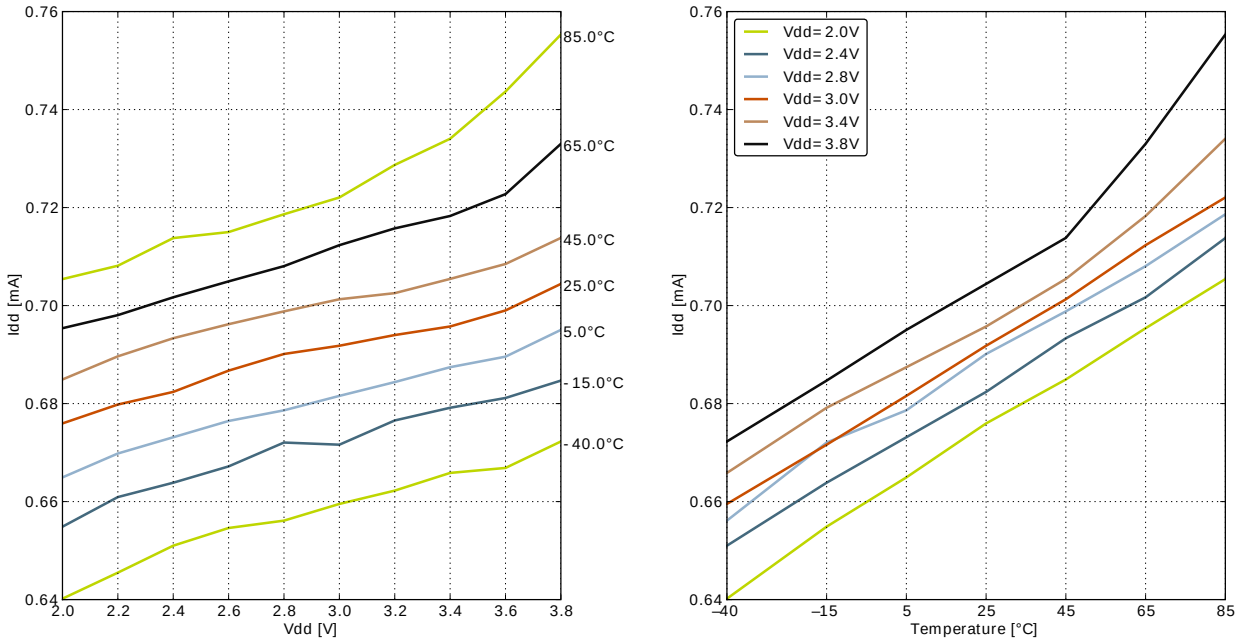


Figure 3.9. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 11MHz

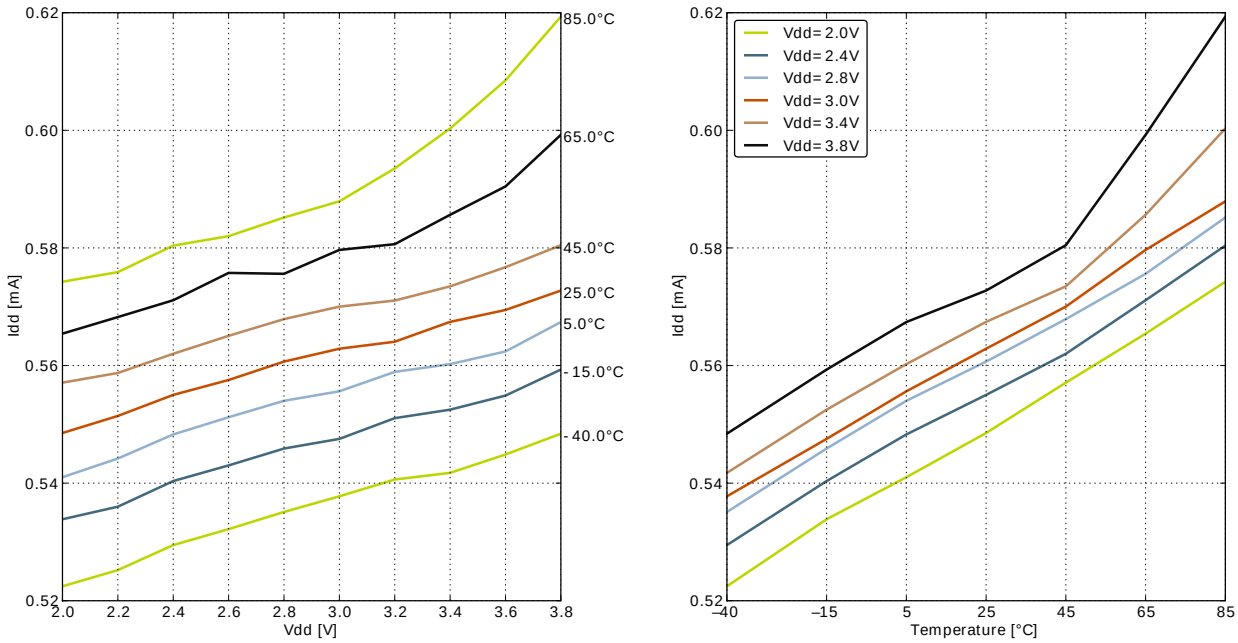


Figure 3.10. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 7MHz

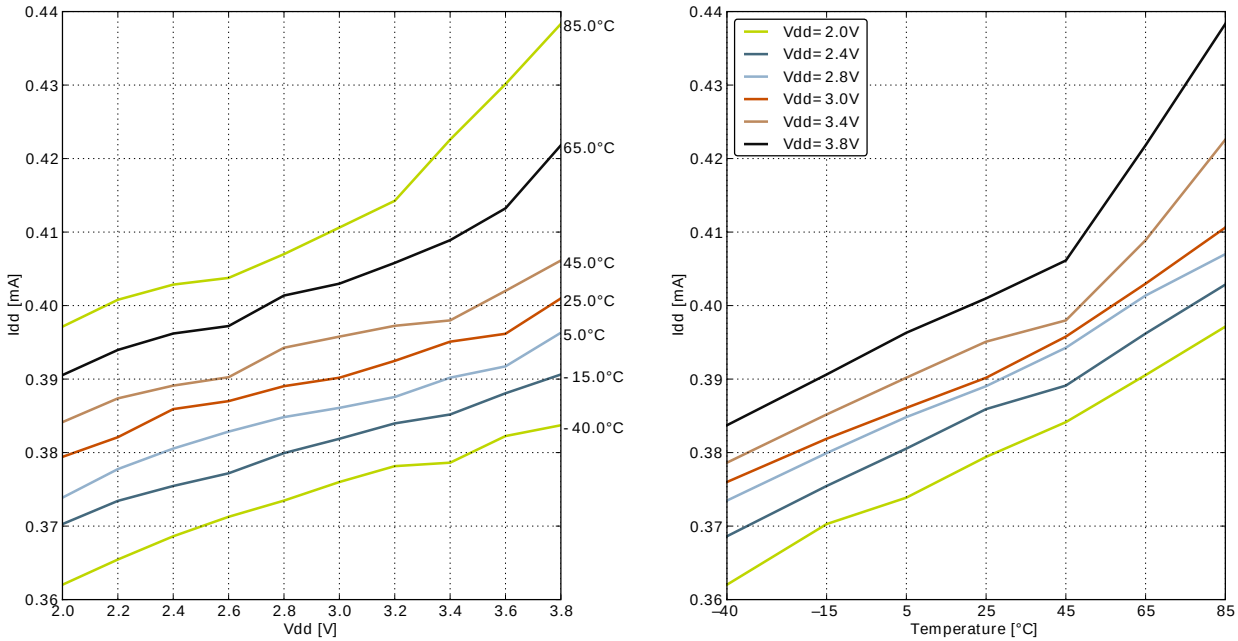


Figure 3.11. EM2 current consumption. RTC prescaled to 1kHz, 32 kHz LFRCO.

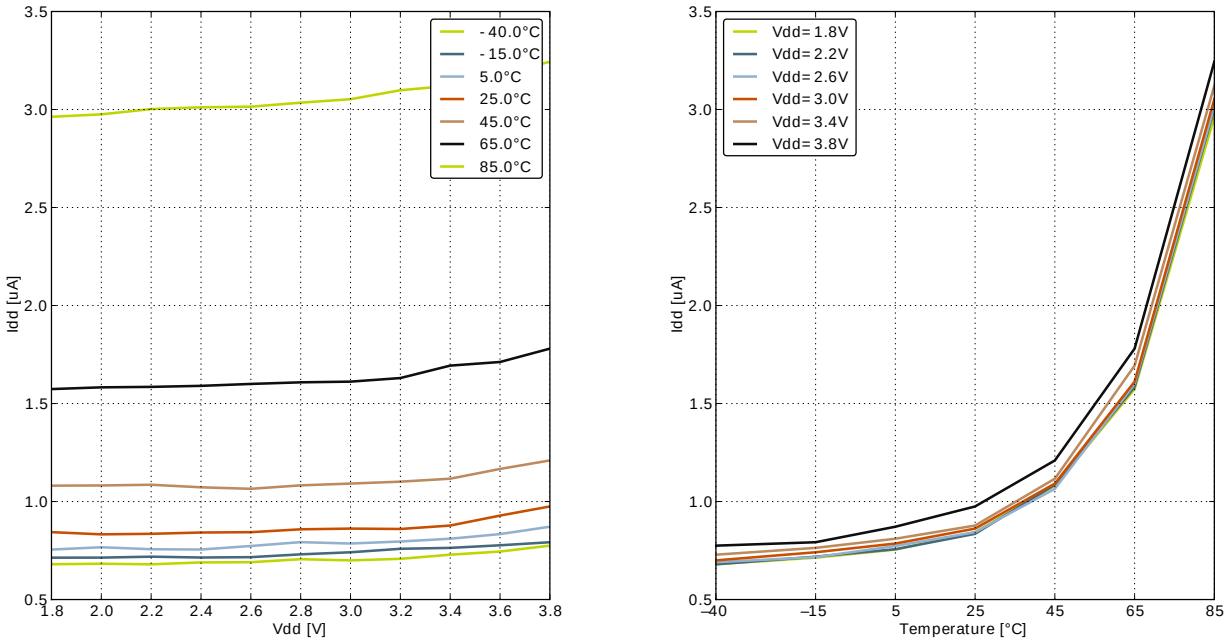


Figure 3.12. EM3 current consumption.

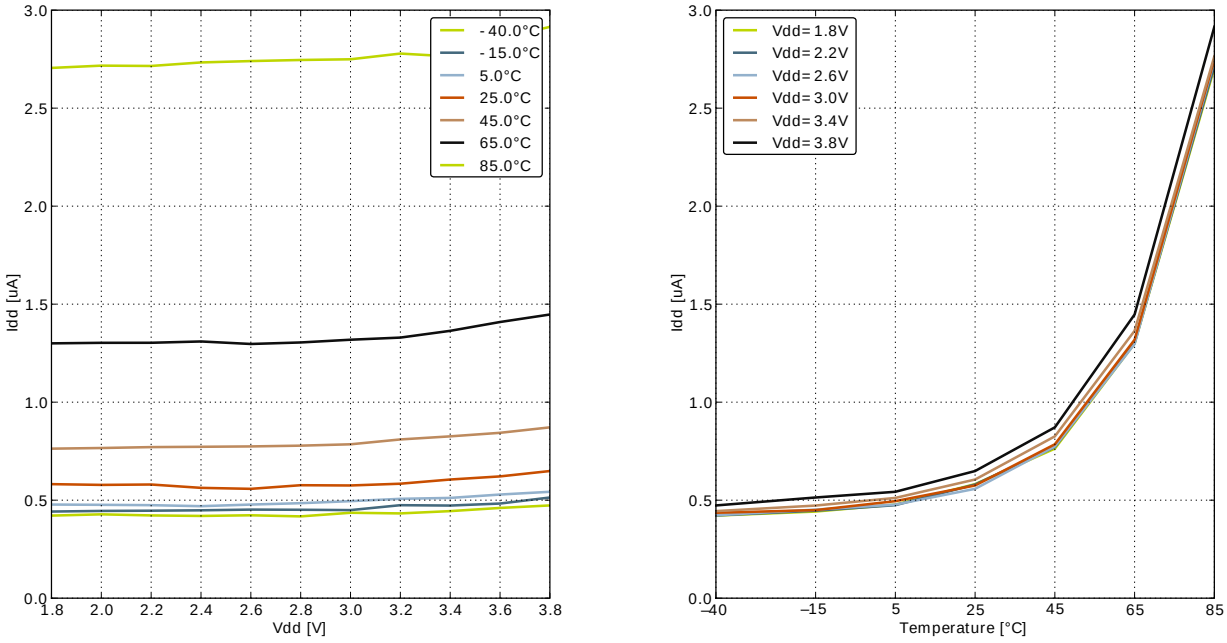
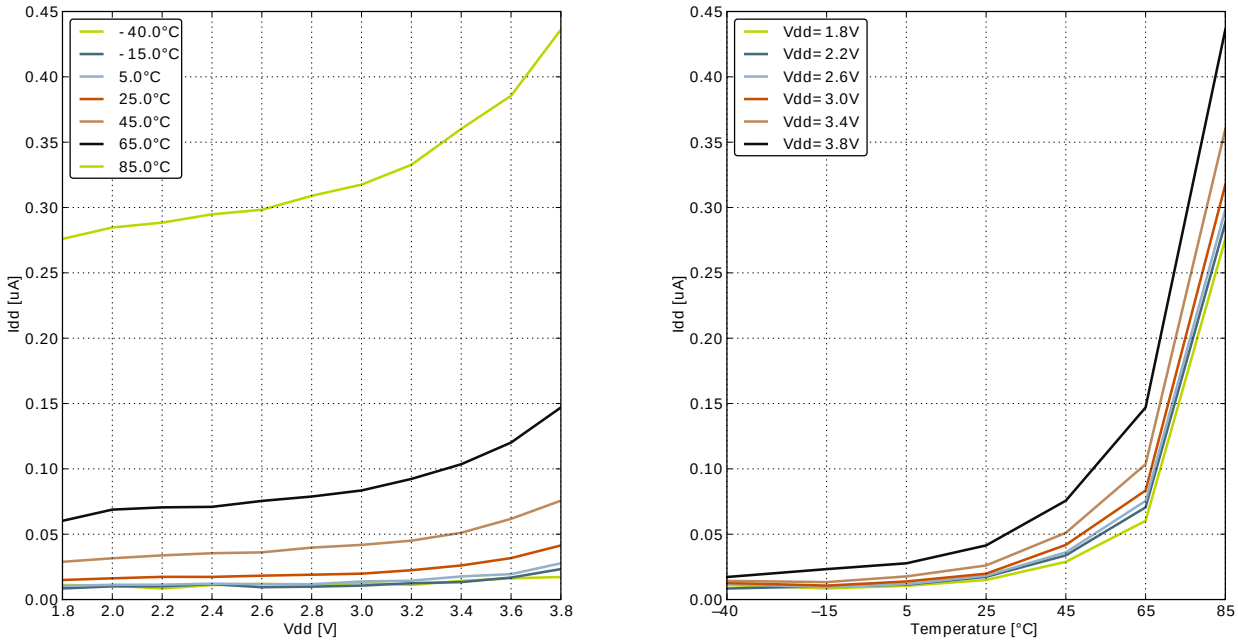


Figure 3.13. EM4 current consumption.



3.5 Transition between Energy Modes

Table 3.5. Energy Modes Transitions

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{EM10}	Transition time from EM1 to EM0			0[1]		HF core CLK cycles
t_{EM20}	Transition time from EM2 to EM0			2		µs
t_{EM30}	Transition time from EM3 to EM0			2		µs
t_{EM40}	Transition time from EM4 to EM0			163		µs

[1]Core wakeup time only.

3.6 Power Management

Table 3.6. Power Management

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{BODextthr-}$	BOD threshold on falling external supply voltage		1.77		1.80	V
$V_{BODintthr-}$	BOD threshold on falling internally regulated supply voltage		1.62		1.65	V
$V_{BODextthr+}$	BOD threshold on rising external supply voltage	Uncalibrated		1.82		V
$V_{BODexthyst}$	BOD hysteresis on external supply voltage			150		mV
TC_{BGR}	Temperature coefficient of band-gap reference (BGR)	Relative voltage variation in EM0 based on the difference in V_{ref} between -40°C and 85°C.			0.55	%
t_{RESET}	Delay from reset is released until program execution starts	Applies to Power-on Reset, Brown-out Reset and pin reset.		163		µs
$C_{DECOUPLE}$	Voltage regulator decoupling capacitor.	X5R capacitor recommended. Apply between DECOUPLE pin and GROUND		1		µF

3.7 Flash

Table 3.7. Flash

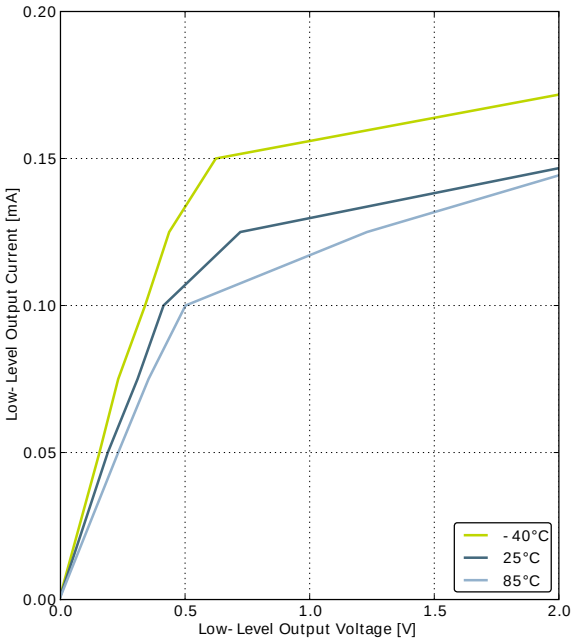
Symbol	Parameter	Condition	Min	Typ	Max	Unit
EC_{FLASH}	Flash erase cycles before failure		20000			cycles
RET_{FLASH}	Flash data retention	T_{AMB}<85°C	10			years
t_{W_PROG}	Word (32-bit) programming time		20			µs
t_{P_ERASE}	Page erase time		20	20.4	20.8	ms
t_{D_ERASE}	Device erase time		40	40.8	41.6	ms

3.8 General Purpose Input Output

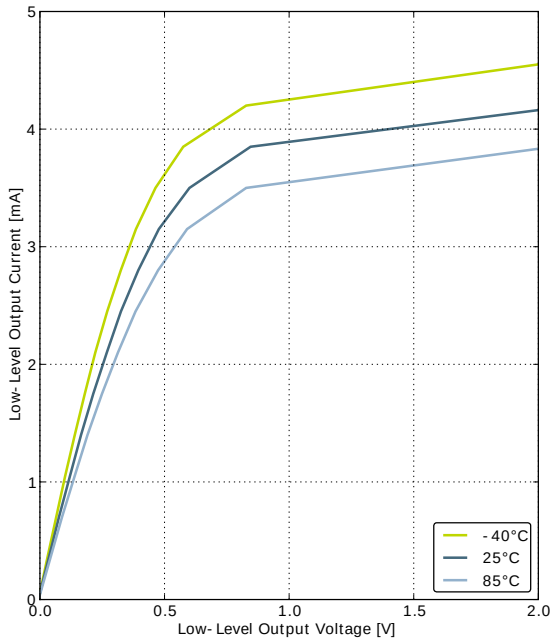
Table 3.8. GPIO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IOIL}	Input low voltage				0.3V_{DD}	V
V_{IOIH}	Input high voltage		0.7V_{DD}			V
V_{IOOH}	Output high voltage relative to V_{DD}	Sourcing 6 mA, V_{DD}=1.8V	75			%
		Sourcing 6 mA, V_{DD}=3.0V	95			%
		Sourcing 20 mA, V_{DD}=1.8V	70			%
		Sourcing 20 mA, V_{DD}=3.0V	90			%
V_{IOOL}	Output low voltage relative to V_{DD}	Sinking 6 mA, V_{DD}=1.8V			25	%
		Sinking 6 mA, V_{DD}=3.0V			5	%
		Sinking 20 mA, V_{DD}=1.8V			30	%
		Sinking 20 mA, V_{DD}=3.0V			10	%
R_{PU}	I/O pin pull-up resistor			40		kOhm
R_{PD}	I/O pin pull-down resistor			40		kOhm
R_{IOESD}	Internal ESD series resistor			200		Ohm
$t_{IOGLITCH}$	Pulse width of pulses to be removed by the glitch suppression filter		10		50	ns
t_{IOOF}	Output fall time	0.5 mA drive strength and load capacitance C_L=12.5-25pF.	20+0.1C_L		250	ns
		2mA drive strength and load capacitance C_L=350-600pF	20+0.1C_L		250	ns
V_{IOHYST}	I/O pin hysteresis (V_{IOTHR+} - V_{IOTHR-})	V_{DD} = 1.8 - 3.8 V	0.1V_{DD}			V

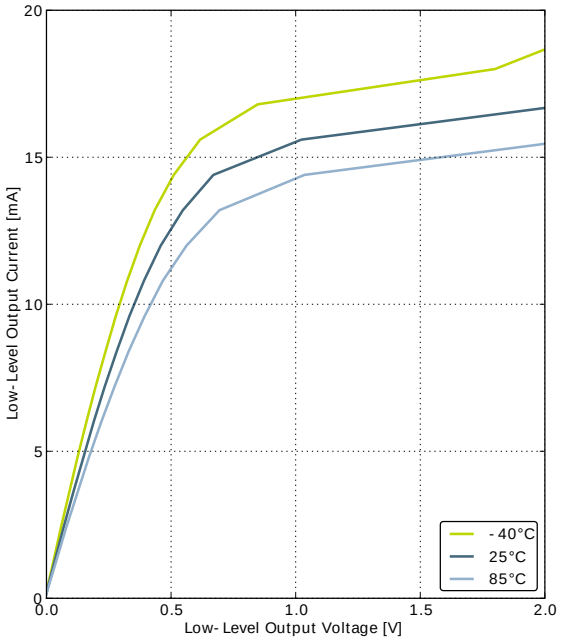
Figure 3.14. Typical Low-Level Output Current, 2V Supply Voltage



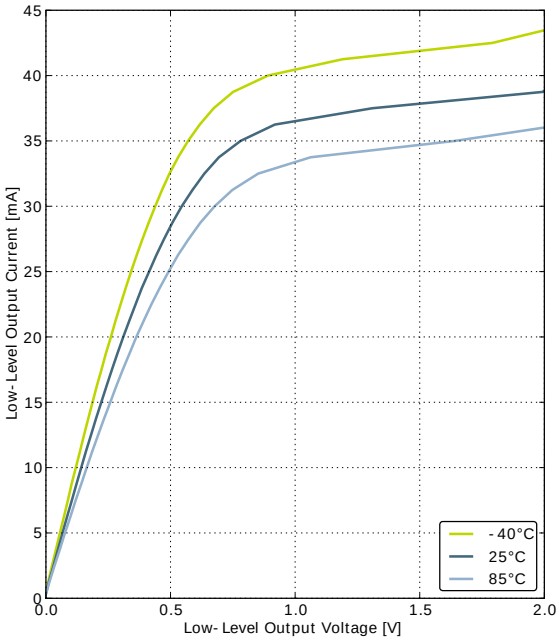
GPIO_Px_CTRL Drive Mode = LOWEST



GPIO_Px_CTRL Drive Mode = LOW

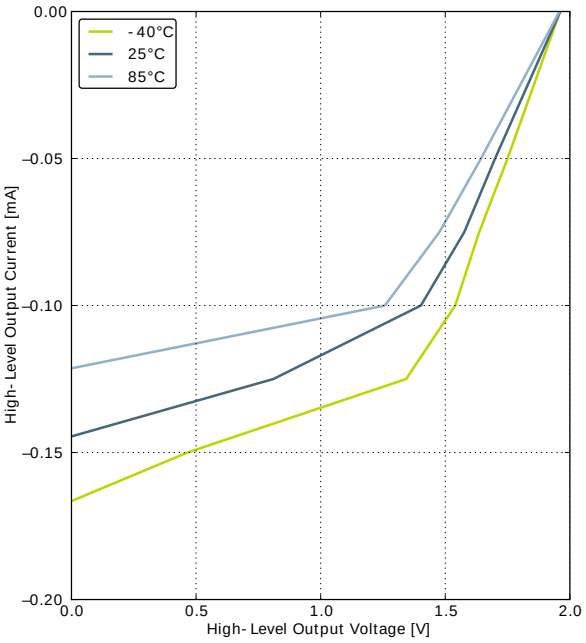


GPIO_Px_CTRL Drive Mode = STANDARD

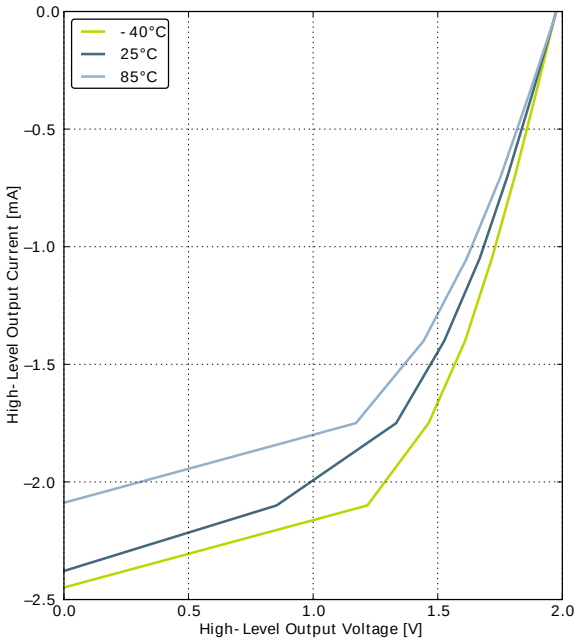


GPIO_Px_CTRL Drive Mode = HIGH

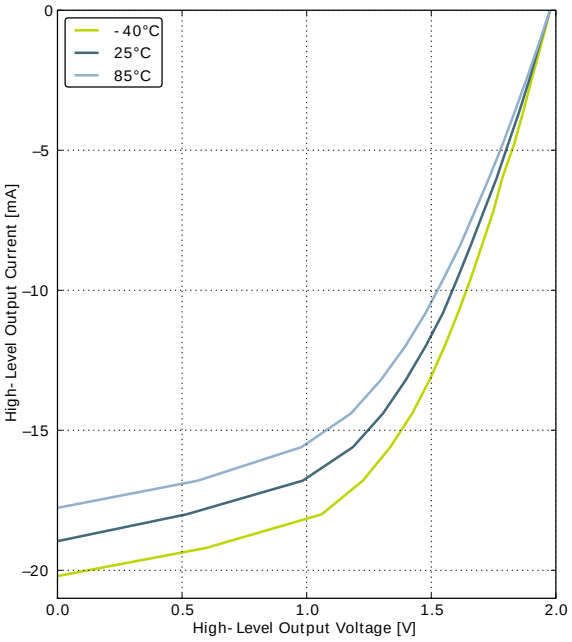
Figure 3.15. Typical High-Level Output Current, 2V Supply Voltage



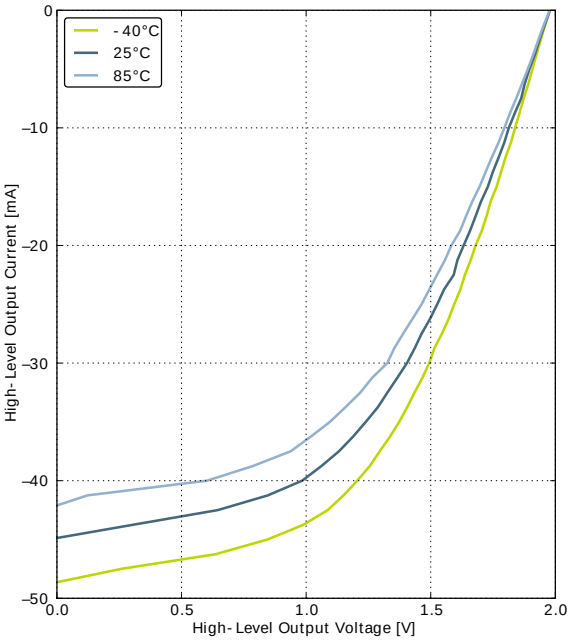
GPIO_Px_CTRL Drive Mode = LOWEST



GPIO_Px_CTRL Drive Mode = LOW

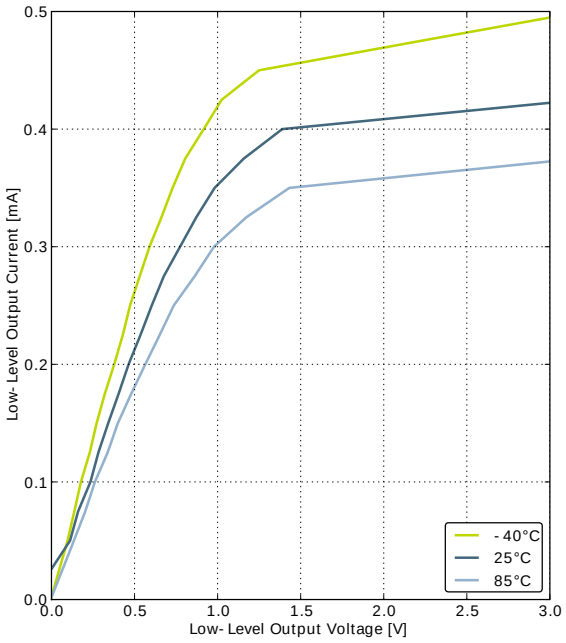


GPIO_Px_CTRL Drive Mode = STANDARD

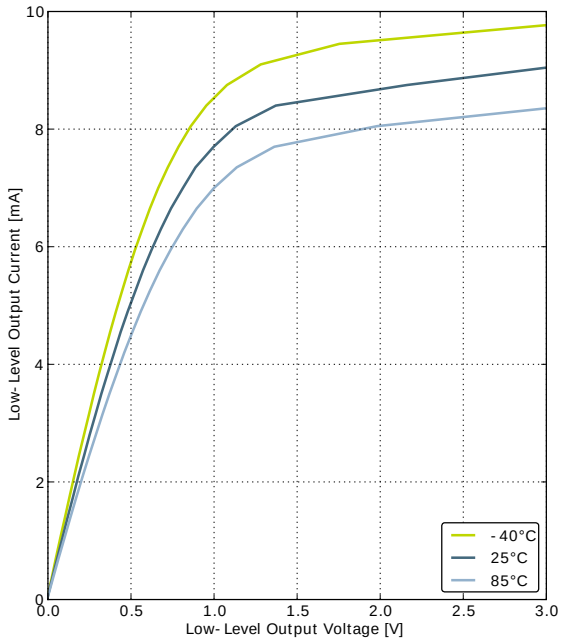


GPIO_Px_CTRL Drive Mode = HIGH

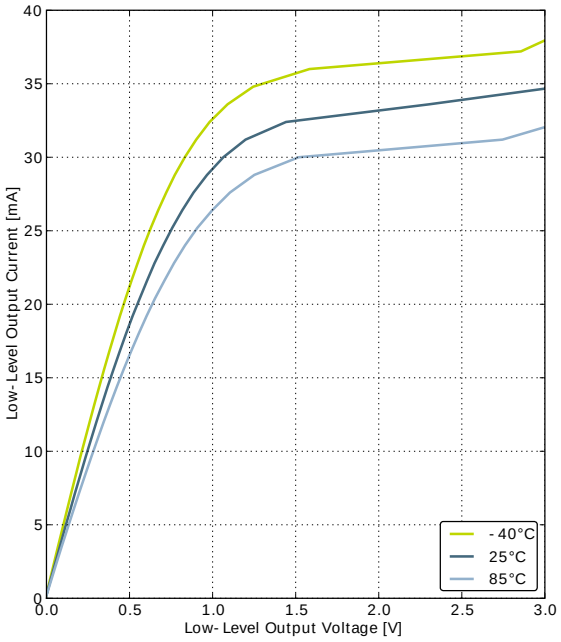
Figure 3.16. Typical Low-Level Output Current, 3V Supply Voltage



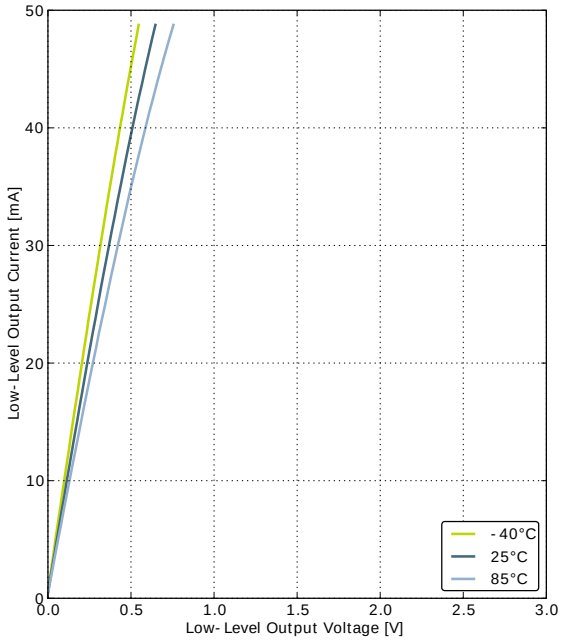
GPIO_Px_CTRL Drive Mode = LOWEST



GPIO_Px_CTRL Drive Mode = LOW

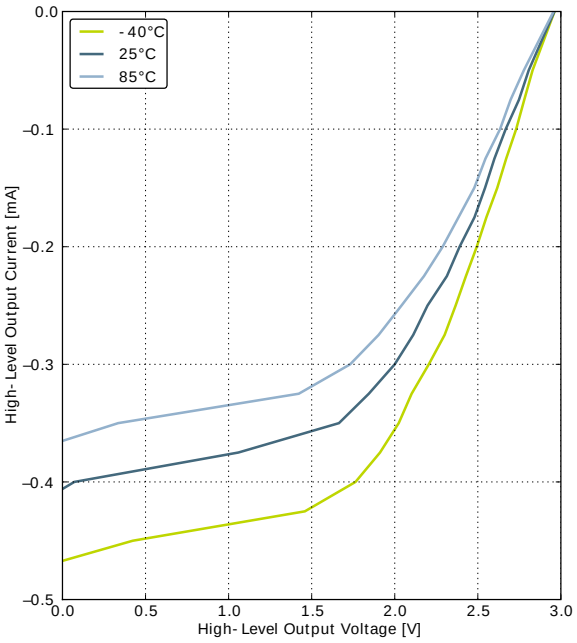


GPIO_Px_CTRL Drive Mode = STANDARD

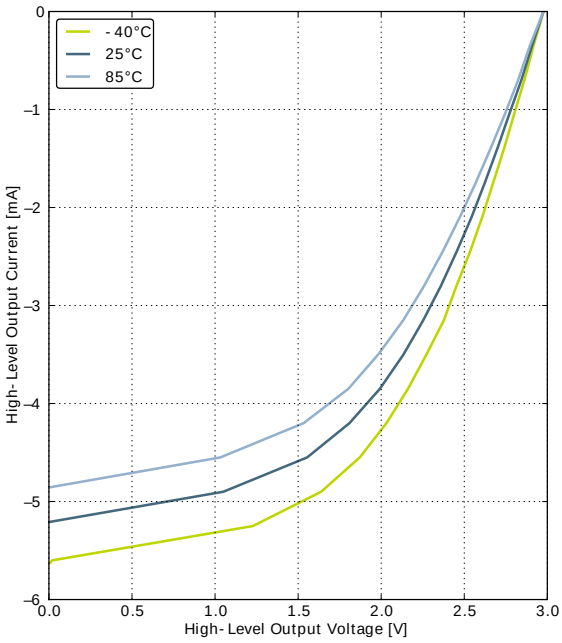


GPIO_Px_CTRL Drive Mode = HIGH

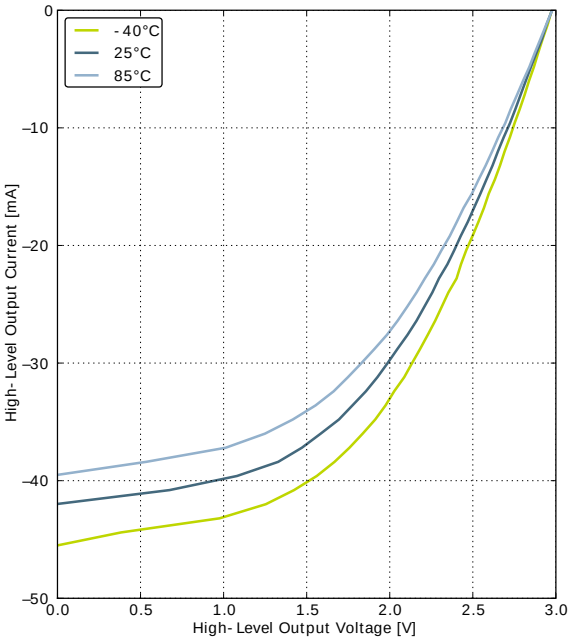
Figure 3.17. Typical High-Level Output Current, 3V Supply Voltage



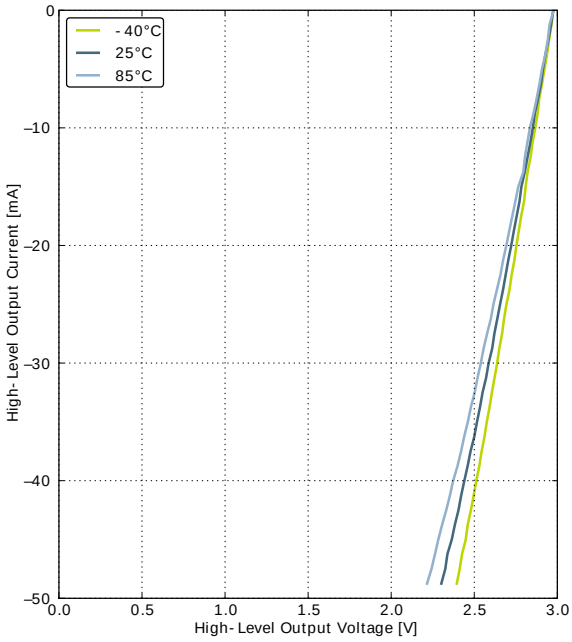
GPIO_Px_CTRL Drive Mode = LOWEST



GPIO_Px_CTRL Drive Mode = LOW

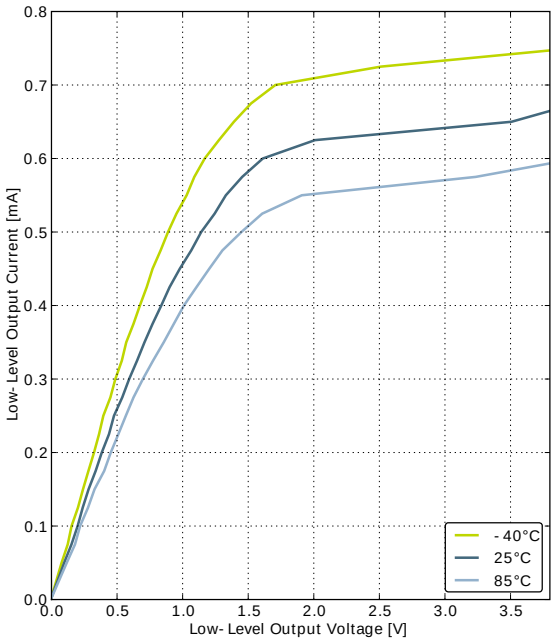


GPIO_Px_CTRL Drive Mode = STANDARD

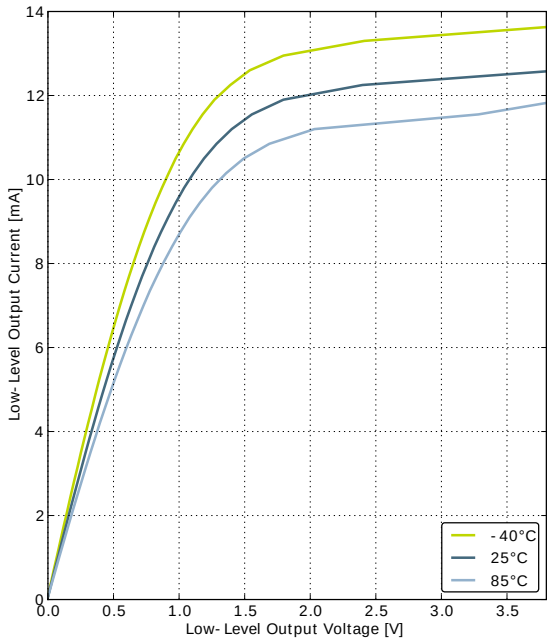


GPIO_Px_CTRL Drive Mode = HIGH

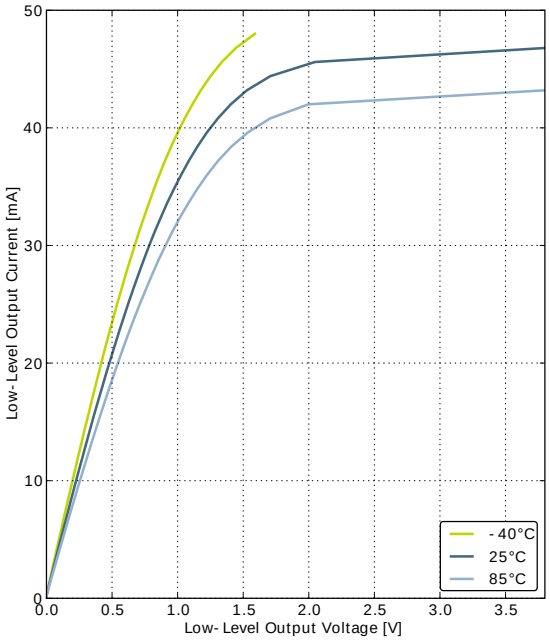
Figure 3.18. Typical Low-Level Output Current, 3.8V Supply Voltage



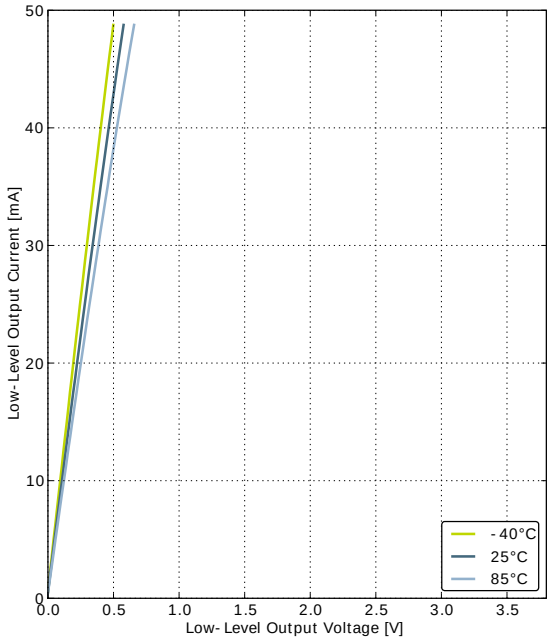
GPIO_Px_CTRL Drive Mode = LOWEST



GPIO_Px_CTRL Drive Mode = LOW

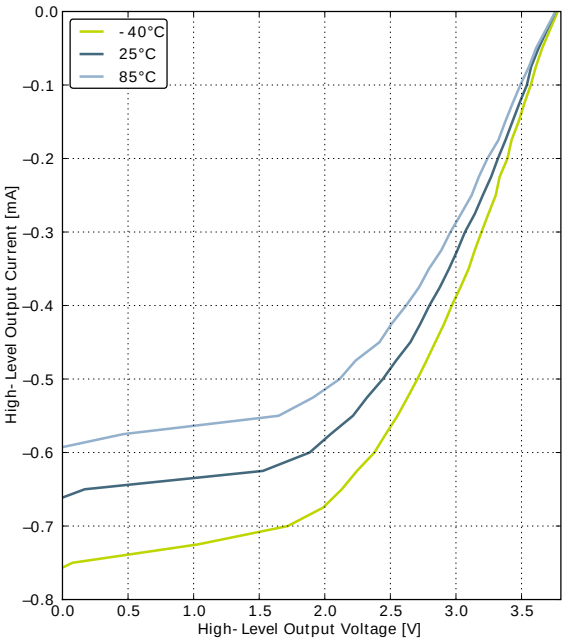


GPIO_Px_CTRL Drive Mode = STANDARD

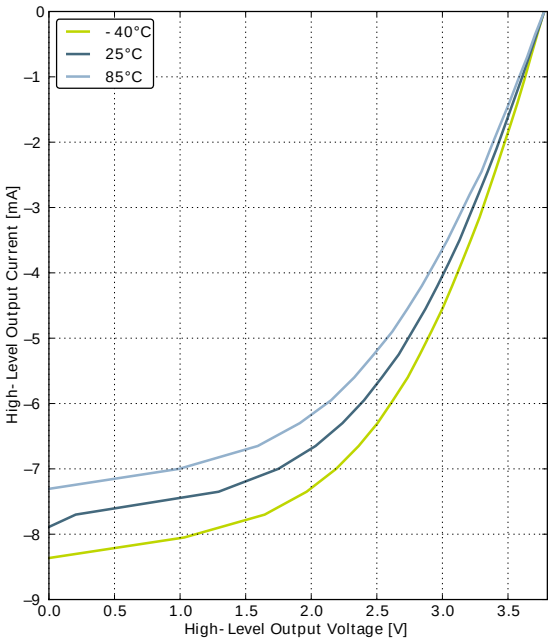


GPIO_Px_CTRL Drive Mode = HIGH

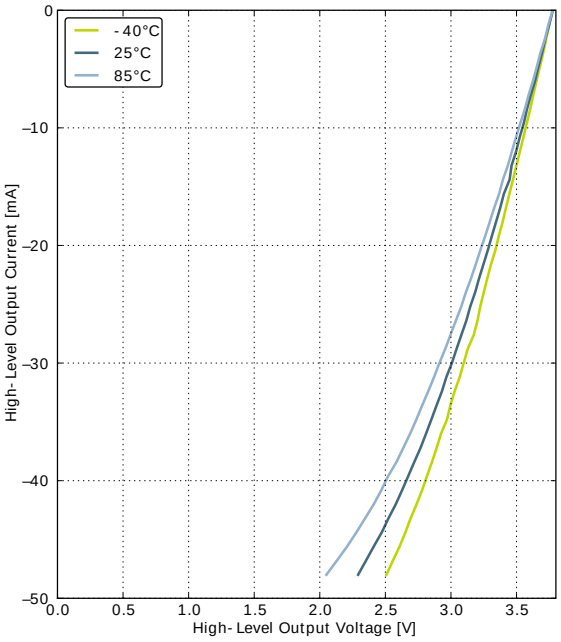
Figure 3.19. Typical High-Level Output Current, 3.8V Supply Voltage



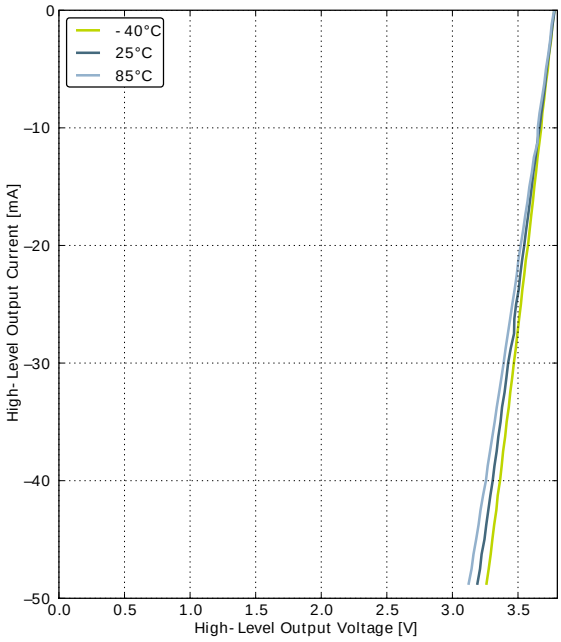
GPIO_Px_CTRL Drive Mode = LOWEST



GPIO_Px_CTRL Drive Mode = LOW



GPIO_Px_CTRL Drive Mode = STANDARD



GPIO_Px_CTRL Drive Mode = HIGH

3.9 Oscillators

3.9.1 LFXO

Table 3.9. LFXO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{LFXO}	Crystal frequency			32.768		kHz
ESR_{LFXO}	Supported crystal equivalent series resistance (ESR)			30	120	kOhm
C_{LFXOL}	Supported crystal external load range		5		25	pF
DC_{LFXO}	Duty cycle		48	50	53.5	%
I_{LFXO}	Current consumption for core and buffer after start-up.	ESR=30 kOhm, C_L=10 pF, LFXOBOOST in CMU_CTRL is 1		190		nA
t_{LFXO}	Start- up time.	ESR=30 kOhm, C_L=10 pF, 40% - 60% duty cycle has been reached, LFXOBOOST in CMU_CTRL is 1		400		ms

3.9.2 HFXO

Table 3.10. HFXO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{HFXO}	Crystal Frequency		4		32	MHz
ESR_{HFXO}	Supported crystal equivalent series resistance (ESR)	Crystal frequency 32 MHz		30	60	Ohm
		Crystal frequency 4 MHz		400	1500	Ohm
g_{mHFXO}	The transconductance of the HFXO input transistor at crystal startup	HFXOBOOST in CMU_CTRL equals 0b11	20			mS
C_{HFXOL}	Supported crystal external load range		5		25	pF
DC_{HFXO}	Duty cycle		46	50	54	%
I_{HFXO}	Current consumption for HFXO after startup	4 MHz: ESR=400 Ohm, C_L=20 pF, HFXOBOOST in CMU_CTRL equals 0b11		85		µA
		32 MHz: ESR=30 Ohm, C_L=10 pF, HFXOBOOST in CMU_CTRL equals 0b11		165		µA
t_{HFXO}	Startup time	32 MHz: ESR=30 Ohm, C_L=10 pF, HFXOBOOST in CMU_CTRL equals 0b11		400		µs

3.9.3 LFRCO

Table 3.11. LFRCO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{LFRCO}	Oscillation frequency			32		kHz
t_{LFRCO}	Startup time not including software calibration			150		µs
I_{LFRCO}	Current consumption			190		nA
$TUNESTEP_{L-FRCO}$	Frequency step for LSB change in TUNING value			1.5		%

3.9.4 HFRCO

Table 3.12. HFRCO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{HFRCO}	Oscillation frequency	28 MHz frequency band		28		MHz
		21 MHz frequency band		21		MHz
		14 MHz frequency band		14		MHz
		11 MHz frequency band		11		MHz
		7 MHz frequency band		7		MHz
		1 MHz frequency band		1		MHz
t_{HFRCO}	Start-up time not including software calibration	f_{HFRCO} = 14 MHz		0.6		µs
I_{HFRCO}	Current consumption	f_{HFRCO} = 28 MHz		106		µA
		f_{HFRCO} = 21 MHz		93		µA
		f_{HFRCO} = 14 MHz		77		µA
		f_{HFRCO} = 11 MHz		72		µA
		f_{HFRCO} = 7 MHz		63		µA
DC_{HFRCO}	Duty cycle	f_{HFRCO} = 14 MHz	48.5	50	51	%
$TUNESTEP_{H-FRCO}$	Frequency step for LSB change in TUNING value			0.3		%

3.9.5 ULFRCO

Table 3.13. ULFRCO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{ULFRCO}	Oscillation frequency	25°C, 3V	0.8		1.5	kHz
TC_{ULFRCO}	Temperature coefficient			0.05		%/°C
VC_{ULFRCO}	Supply voltage coefficient			-18.2		%/V

3.10 Analog Digital Converter (ADC)

Table 3.14. ADC

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{ADCCM}	Analog input common mode voltage range		0		V_{DD}	V
V_{ADCIN}	Input voltage range of external reference voltage, single ended and differential		1.25		V_{DD}	V
I_{ADC}	Average active current	1 MSamples/s, 12 bit, external reference		220		µA
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUPMODE in ADCn_CTRL set to 0b00		9		µA
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUPMODE in ADCn_CTRL set to 0b01		6		µA
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUPMODE in ADCn_CTRL set to 0b10		74		µA
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUPMODE in ADCn_CTRL set to 0b11		290		µA
		6 bit 10 kSamples/s, internal 1.25 V reference, WARMUPMODE in ADCn_CTRL set to 0b01		4		µA
I_{ADCREF}	Current consumption of internal voltage reference	Internal voltage reference		70		µA
C_{ADCIN}	Input capacitance			2		pF
R_{ADCIN}	Input ON resistance		1			MOhm
$V_{ADCCMOUT}$	Common mode output voltage range			1.65		V
f_{ADCCLK}	Frequency of ADC clock, max and min			13		MHz
$t_{ADCCONV}$	Conversion time			1		µs
t_{ADCACQ}	Acquisition time	Programmable		0.5		µs
$t_{ADCACQVDD3}$	Required sample time for VDD/3 reference			2		µs
$t_{ADCSTART}$	Startup time of reference generator in NORMAL mode and startup time ADC			5		µs
	Startup time of reference generator in KEEPADCWARM mode and startup time ADC			1		µs

Symbol	Parameter	Condition	Min	Typ	Max	Unit
SNR_{ADC}	Signal to Noise Ratio (SNR)	1 MSamples/s, 12 bit, single ended, internal 1.25V reference		69		dB
		1 MSamples/s, 12 bit, single ended, internal 2.5V reference		72		dB
		1 MSamples/s, 12 bit, differential, internal 1.25V reference		70		dB
		1 MSamples/s, 12 bit, differential, internal 2.5V reference		73		dB
		1 MSamples/s, 12 bit, differential, 5V reference		73		dB
		100 kSamples/s, 12 bit, single ended, internal 1.25V reference		69		dB
		100 kSamples/s, 12 bit, single ended, internal 2.5V reference		72		dB
		100 kSamples/s, 12 bit, differential, internal 1.25V reference		70		dB
		100 kSamples/s, 12 bit, differential, internal 2.5V reference		73		dB
		100 kSamples/s, 12 bit, differential, 5V reference		73		dB
		1.86 MSamples/s, 6 bit, single ended, internal 1.25V reference		37		dB
$SNDR_{ADC}$	Signal to Noise-puls-Distortion Ratio (SNDR)	1 MSamples/s, 12 bit, single ended, internal 1.25V reference		68		dB
		1 MSamples/s, 12 bit, single ended, internal 2.5V reference		71		dB
		1 MSamples/s, 12 bit, differential, internal 1.25V reference		69		dB
		1 MSamples/s, 12 bit, differential, internal 2.5V reference		72		dB
		1 MSamples/s, 12 bit, differential, 5V reference		72		dB
		100 kSamples/s, 12 bit, single ended, internal 1.25V reference		68		dB
		100 kSamples/s, 12 bit, single ended, internal 2.5V reference		71		dB
		100 kSamples/s, 12 bit, differential, internal 1.25V reference		69		dB

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		100 kSamples/s, 12 bit, differential, internal 2.5V reference		72		dB
		100 kSamples/s, 12 bit, differential, 5V reference		72		dB
		1.86 MSamples/s, 6 bit, single ended, internal 1.25V reference		37		dB
$SFDR_{ADC}$	Spurious-Free Dynamic Range (SFDR)	1 MSamples/s, 12 bit, single ended, internal 1.25V reference		75		dB
		1 MSamples/s, 12 bit, single ended, internal 2.5V reference		75		dB
		1 MSamples/s, 12 bit, differential, internal 1.25V reference		75		dB
		1 MSamples/s, 12 bit, differential, internal 2.5V reference		75		dB
		1 MSamples/s, 12 bit, differential, 5V reference		75		dB
		100 kSamples/s, 12 bit, single ended, internal 1.25V reference		75		dB
		100 kSamples/s, 12 bit, single ended, internal 2.5V reference		75		dB
		100 kSamples/s, 12 bit, differential, internal 1.25V reference		75		dB
		100 kSamples/s, 12 bit, differential, internal 2.5V reference		75		dB
		100 kSamples/s, 12 bit, differential, 5V reference		75		dB
		1.86 MSamples/s, 6 bit, single ended, internal 1.25V reference		57		dB
$V_{ADCOFFSET}$	Offset voltage	Before calibration, single ended		10		mV
		After calibration, single ended		0.3		mV
		Before calibration, differential		10		mV
		After calibration, differential		0.3		mV
$TGRAD_{ADCTH}$	Thermometer output gradient			-1.85		mV/°C
				-6.1		ADC Codes/ °C
DNL_{ADC}	Differential non-linearity (DNL)	Internal 1.25V reference		1		LSB
		Internal 2.5V reference		1		LSB
		Internal 5V reference		1		LSB

Symbol	Parameter	Condition	Min	Typ	Max	Unit
INL_{ADC}	Integral non-linearity (INL), End point method	Internal 1.25V reference		2		LSB
		Internal 2.5V reference		2		LSB
		Internal 5V reference		2		LSB
MC_{ADC}	No missing codes	12 bit, internal 1.25V reference, single ended		0		
		12 bit, internal 1.25V reference, differential		0		
		12 bit, internal 2.5V reference, single ended		0		
		12 bit, internal 2.5V reference, differential		0		
		12 bit, internal 5V reference, differential		0		

The integral non-linearity (INL) and differential non-linearity parameters are explained in Figure 3.20 (p. 31) and Figure 3.21 (p. 32) , respectively.

Figure 3.20. Integral Non-Linearity (INL)

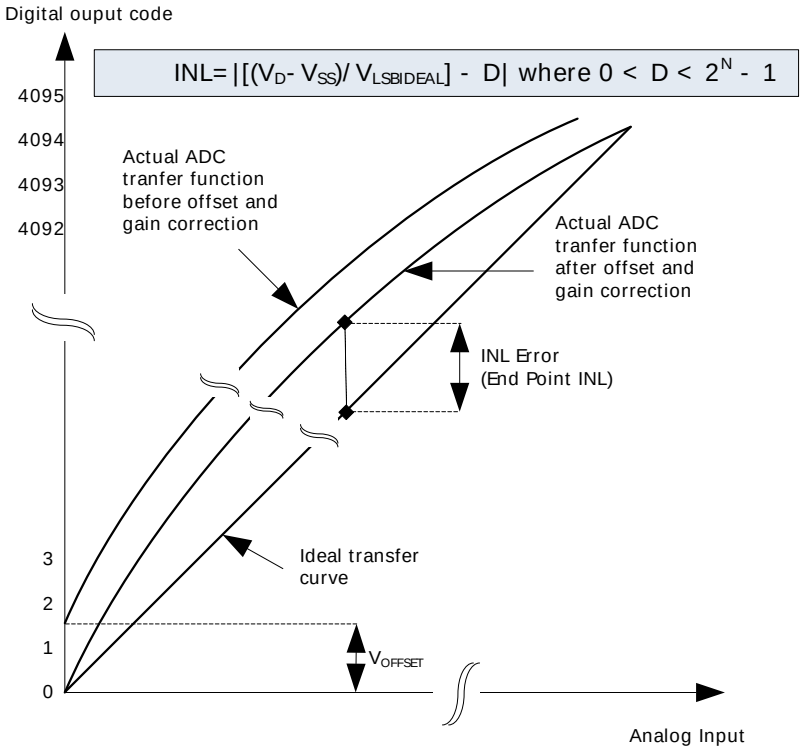
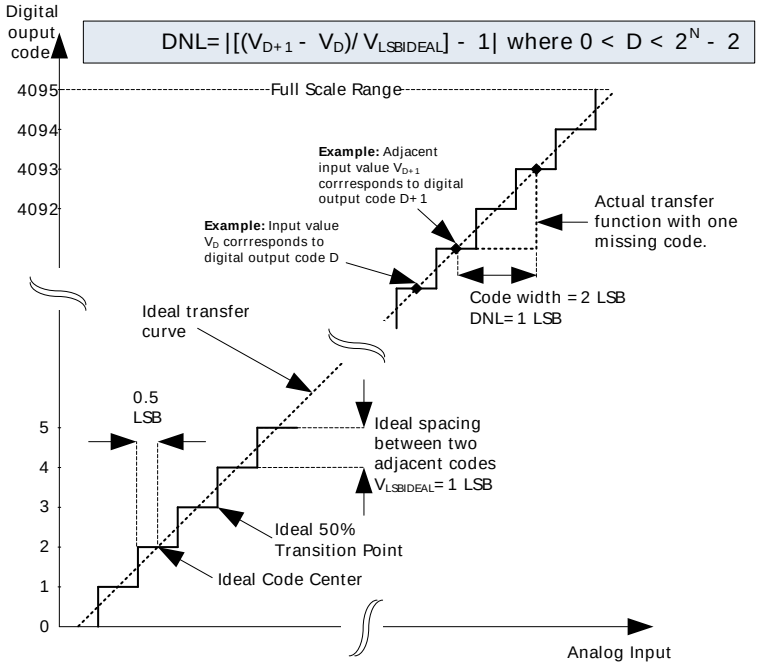


Figure 3.21. Differential Non-Linearity (DNL)



3.11 Digital Analog Converter (DAC)

Table 3.15. DAC

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DACOUT}	Output voltage range	External voltage reference, single ended	0		V_{DD}	V
V_{DACCM}	Output common mode voltage range		0		V_{DD}	V
I_{DAC}	Active current including references for 2 channels	500 kSamples/s, 12bit		400		µA
		100 kSamples/s, 12 bit		200		µA
		1 kSamples/s 12 bit NORMAL		38		µA
SR_{DAC}	DAC sample rate			500		ksamples/s
f_{DAC}	DAC clock frequency			1		MHz
$CYC_{DACCONV}$	Clock cyckles per conversion			2		
$t_{DACCONV}$	DAC conversion time			2		µs
$t_{DACSETTLE}$	DAC settling time			5		µs
SNR_{DAC}	DAC Signal to Noise Ratio (SNR)	500 kSamples/s, 12 bit, single ended, internal 1.25V reference		71		dB
		500 kSamples/s, 12 bit, single ended, internal 2.5V reference		70		dB
		100 kSamples/s, 12 bit, single ended, internal 1.25V reference		72		dB

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		100 kSamples/s, 12 bit, single ended, internal 2.5V reference		71		dB
$SNDR_{DAC}$	DAC Signal to Noise-pulse Distortion Ratio (SNDR)	500 kSamples/s, 12 bit, single ended, internal 1.25V reference		70		dB
		500 kSamples/s, 12 bit, single ended, internal 2.5V reference		69		dB
		100 kSamples/s, 12 bit, single ended, internal 1.25V reference		71		dB
		100 kSamples/s, 12 bit, single ended, internal 2.5V reference		70		dB
$SFDR_{DAC}$	DAC Spurious-Free Dynamic Range(SFDR)	500 kSamples/s, 12 bit, single ended, internal 1.25V reference		75		dB
		500 kSamples/s, 12 bit, single ended, internal 2.5V reference		75		dB
		100 kSamples/s, 12 bit, single ended, internal 1.25V reference		75		dB
		100 kSamples/s, 12 bit, single ended, internal 2.5V reference		75		dB
$V_{DACOFFSET}$	Offset voltage	Before calibration, single ended		10		mV
		After calibration, single ended		0.5		mV
DNL_{DAC}	Differential non-linearity	Internal 1.25V reference		1		LSB
		Internal 2.5V reference		1		LSB
INL_{DAC}	Integral non-linearity	Internal 1.25V reference		2		LSB
		Internal 2.5V reference		2		LSB
MC_{DAC}	No missing codes	12 bit, internal 1.25V reference, single ended		0		
		12 bit, internal 2.5V reference, single ended		0		

3.12 Operational Amplifier (OPAMP)

Table 3.16. OPAMP

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{OPAMP}	Active Current	Lowest Bias Setting		20		µA
		Highest Bias Setting		500		µA
G_{OL}	Open Loop Gain			100		dB
GBW_{OPAMP}	Gain Bandwidth Product			2.2		MHz
R_{LOAD}	Load Resistance			200		Ohm
$CMRR_{OPAMP}$	Common Mode Rejection Ratio			60		dB
$PSRR_{OPAMP}$	Power Supply Rejection Ratio			60		dB

3.13 Analog Comparator (ACMP)

Table 3.17. ACMP

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{ACMPIN}	Input voltage range		0		V_{DD}	V
V_{ACMPCM}	ACMP Common Mode voltage range		0		V_{DD}	V
I_{ACMP}	Active current	BIASPROG=0b0000, FULLBIAS=0 and HALFBIAS=1 in ACMPn_CTRL register		0.1		µA
		BIASPROG=0b1111, FULLBIAS=0 and HALFBIAS=0 in ACMPn_CTRL register		2.87		µA
		BIASPROG=0b1111, FULLBIAS=1 and HALFBIAS=0 in ACMPn_CTRL register		195		µA
$I_{ACMPREF}$	Current consumption of internal voltage reference	Internal voltage reference off. Using external voltage reference		0		µA
		Internal voltage reference		5		µA
$V_{ACMPOFFSET}$	Offset voltage	Single ended		10		mV
		Differential		10		mV
$V_{ACMPHYST}$	ACMP hysteresis	Programmable		17		mV
R_{CSRES}	Capacitive Sense Internal Resistance	CSRESSEL=0b00 in ACMPn_INPUTSEL		39		kOhm
		CSRESSEL=0b01 in ACMPn_INPUTSEL		71		kOhm
		CSRESSEL=0b10 in ACMPn_INPUTSEL		104		kOhm
		CSRESSEL=0b11 in ACMPn_INPUTSEL		136		kOhm

The total ACMP current is the sum of the contributions from the ACMP and its internal voltage reference as given in Equation 3.1 (p. 35) . $I_{ACMPREF}$ is zero if an external voltage reference is used.

Total ACMP Active Current

$$I_{ACMPTOTAL} = I_{ACMP} + I_{ACMPREF} \quad (3.1)$$

3.14 Voltage Comparator (VCMP)

Table 3.18. VCMP

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{VCMPIN}	Input voltage range			V_{DD}		V
V_{VCMPCM}	VCMP Common Mode voltage range			V_{DD}		V
I_{VCMP}	Active current	BIASPROG=0b0000 and HALFBIAS=1 in VCMPn_CTRL register		0.1		µA
		BIASPROG=0b1111 and HALFBIAS=0 in VCMPn_CTRL register		2.7		µA
$t_{VCMPREF}$	Startup time reference generator	NORMAL		10		µs
$V_{VCMPOFFSET}$	Offset voltage	Single ended		10		mV
		Differential		10		mV
$V_{VCMPHYST}$	VCMP hysteresis			17		mV

The V_{DD} trigger level can be configured by setting the TRIGLEVEL field of the VCMP_CTRL register in accordance with the following equation:

VCMP Trigger Level as a Function of Level Setting

$$V_{DD\ Trigger\ Level} = 1.667V + 0.034 \times TRIGLEVEL \quad (3.2)$$

3.15 Digital Peripherals

Table 3.19. Digital Peripherals

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{USART}	USART current	USART idle current, clock enabled		7.5		µA/MHz
I_{UART}	UART current	UART idle current, clock enabled		5.63		µA/MHz
I_{LEUART}	LEUART current	LEUART idle current, clock enabled		150		nA
I_{I2C}	I2C current	I2C idle current, clock enabled		6.25		µA/MHz
I_{TIMER}	TIMER current	TIMER_0 idle current, clock enabled		8.75		µA/MHz
$I_{LETIMER}$	LETIMER current	LETIMER idle current, clock enabled		150		nA
I_{PCNT}	PCNT current	PCNT idle current, clock enabled		100		nA
I_{RTC}	RTC current	RTC idle current, clock enabled		100		nA

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{AES}	AES current	AES idle current, clock enabled		2.5		µA/MHz
I_{GPIO}	GPIO current	GPIO idle current, clock enabled		5.31		µA/MHz
I_{PRS}	PRS current	PRS idle current		2,81		µA/MHz
I_{DMA}	DMA current	Clock enable		8.12		µA/MHz

4 Pinout and Package

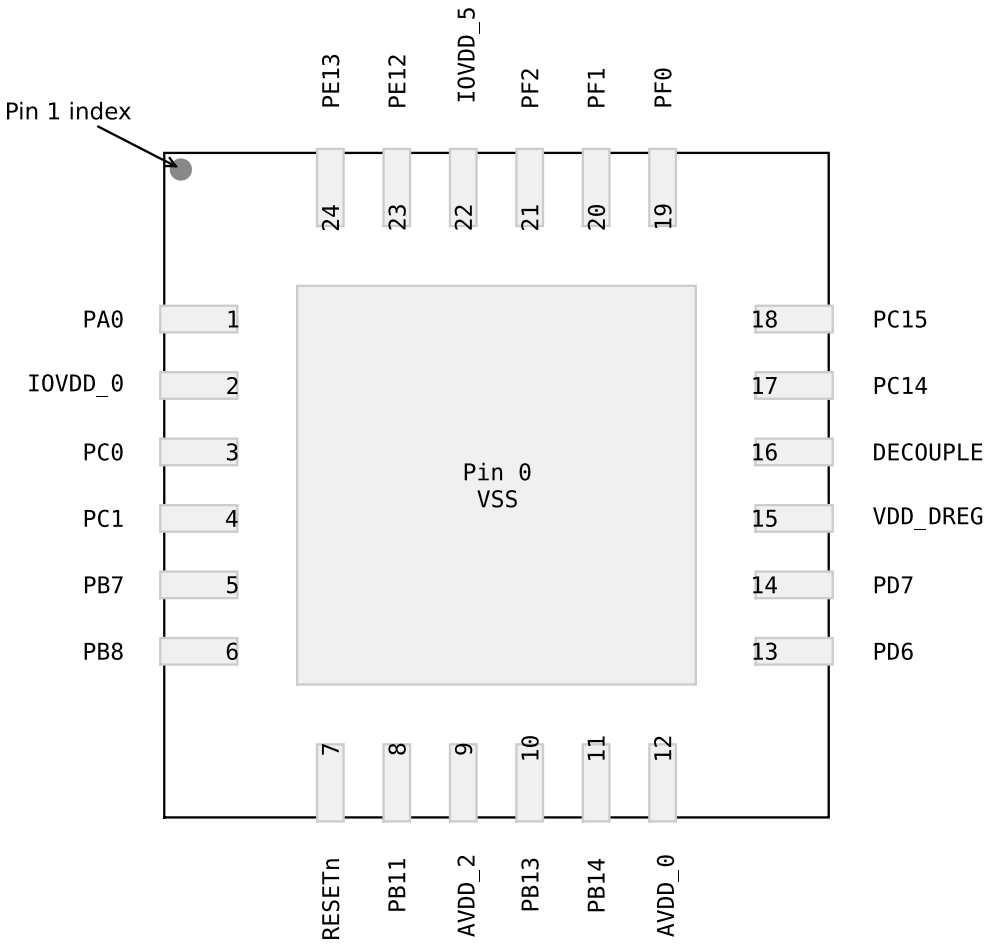
Note

Please refer to the application note "AN0002 EFM32G Hardware Design Considerations" for guidelines on designing Printed Ciruit Boards (PCBs) for the EFM32TG110.

4.1 Pinout

The *EFM32TG110* pinout is shown in Figure 4.1 (p. 37) and Table 4.1 (p. 37). Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

Figure 4.1. EFM32TG110 Pinout (top view, not to scale)



Note

OPAMP output has the same location as DAC0. OPAMP input will be present in later versions of this document.

Table 4.1. Device Pinout

QFN24 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	Debug	Timers	Communication	Other
0	VSS	Ground				

QFN24 Pin# and Name		Pin Alternate Functionality / Description									
Pin #	Pin Name	Analog	Debug	Timers			Communication			Other	
1	PA0	-	-	TIM0_CC0 #0/1/4	-	-	LEU0_RX #4	I2C0_SDA #0	-	-	-
2	IOVDD_0	Digital IO power supply 0.									
3	PC0	ACMP0_CH0	-	TIM0_CC1 #4	PCNT0_S0IN #2	-	US0_TX #5	US1_TX #0	I2C0_SDA #4	-	-
4	PC1	ACMP0_CH1	-	TIM0_CC2 #4	PCNT0_S1IN #2	-	US0_RX #5	US1_RX #0	I2C0_SCL #4	-	-
5	PB7	LFXTAL_P	-	TIM1_CC0 #3	-	-	US0_TX #4	US1_CLK #0	-	-	-
6	PB8	LFXTAL_N	-	TIM1_CC1 #3	-	-	US0_RX #4	US1_CS #0	-	-	-
7	RESETn	Reset input. Active low, with internal pull-up.									
8	PB11	DAC0_OUT0	-	TIM1_CC2 #3	LETIM0_OUT0 #1	-	-	-	-	-	-
9	AVDD_2	Analog power supply 2 .									
10	PB13	HFXTAL_P	-	-	-	-	US0_CLK #4/5	LEU0_TX #1	-	-	-
11	PB14	HFXTAL_N	-	-	-	-	US0_CS #4/5	LEU0_RX #1	-	-	-
12	AVDD_0	Analog power supply 0.									
13	PD6	ADC0_CH6	-	TIM1_CC0 #4	LETIM0_OUT0 #0	PCNT0_S0IN #3	US1_RX #2	I2C0_SDA #1	-	ACMP0_O #2	-
14	PD7	ADC0_CH7	-	TIM1_CC1 #4	LETIM0_OUT1 #0	PCNT0_S1IN #3	US1_TX #2	I2C0_SCL #1	-	CMU_OUT0 #2	ACMP1_O #2
15	VDD_DREG	Power supply for on-chip voltage regulator.									
16	DECOU-PLE	Decouple output for on-chip voltage regulator, nominally at 1.8 V. An external capacitance of size $C_{DECOUPLE}$ is required at this pin.									
17	PC14	ACMP1_CH6	-	TIM1_CC1 #0	PCNT0_S1IN #0	-	US0_CS #3	-	-	-	-
18	PC15	ACMP1_CH7	DBG_SWO #1	TIM1_CC2 #0	-	-	US0_CLK #3	-	-	-	-
19	PF0	-	DBG_SWCLK #0/1	TIM0_CC0 #5	LETIM0_OUT0 #2	-	US1_CLK #2	LEU0_TX #3	I2C0_SDA #5	-	-
20	PF1	-	DBG_SWDIO #0/1	TIM0_CC1 #5	LETIM0_OUT1 #2	-	US1_CS #2	LEU0_RX #3	I2C0_SCL #5	-	-
21	PF2	-	DBG_SWO #0	TIM0_CC2 #5	-	-	LEU0_TX #4	-	-	ACMP1_O #0	-
22	IOVDD_5	Digital IO power supply 5.									
23	PE12	-	-	TIM1_CC2 #1	-	-	US0_RX #3	US0_CLK #0	I2C0_SDA #6	CMU_OUT1 #2	-
24	PE13	-	-	-	-	-	US0_TX #3	US0_CS #0	I2C0_SCL #6	ACMP0_O #0	-

4.2 Alternate functionality pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in Table 4.2 (p. 39). The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note

Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Note

OPAMP output has the same location as DAC0. OPAMP input will be present in later versions of this document.

Table 4.2. Alternate functionality overview

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
ACMP0_CH0	PC0							Analog comparator ACMP0, channel 0.
ACMP0_CH1	PC1							Analog comparator ACMP0, channel 1.
ACMP0_O	PE13		PD6					Analog comparator ACMP0, digital output.
ACMP1_CH6	PC14							Analog comparator ACMP1, channel 6.
ACMP1_CH7	PC15							Analog comparator ACMP1, channel 7.
ACMP1_O	PF2		PD7					Analog comparator ACMP1, digital output.
ADC0_CH6	PD6							Analog to digital converter ADC0, input channel number 6.
ADC0_CH7	PD7							Analog to digital converter ADC0, input channel number 7.
CMU_OUT0			PD7					Clock Management Unit, clock output number 0.
CMU_OUT1			PE12					Clock Management Unit, clock output number 1.
DAC0_OUT0	PB11							Digital to Analog Converter DAC0 output channel number 0.
DBG_SWCLK	PF0	PF0						Debug-interface Serial Wire clock input. Note that this function is enabled to pin out of reset, and has a built-in pull down.
DBG_SWDIO	PF1	PF1						Debug-interface Serial Wire data input / output. Note that this function is enabled to pin out of reset, and has a built-in pull up.
DBG_SWO	PF2	PC15						Debug-interface Serial Wire viewer Output. Note that this function is not enabled after reset, and must be enabled by software to be used.
HFXTAL_N	PB14							High Frequency Crystal (4 - 32 MHz) negative pin. Also used as external optional clock input pin.
HFXTAL_P	PB13							High Frequency Crystal (4 - 32 MHz) positive pin.
I2C0_SCL		PD7			PC1	PF1	PE13	I2C0 Serial Clock Line input / output.
I2C0_SDA	PA0	PD6			PC0	PF0	PE12	I2C0 Serial Data input / output.
LETIM0_OUT0	PD6	PB11	PF0					Low Energy Timer LETIM0, output channel 0.
LETIM0_OUT1	PD7		PF1					Low Energy Timer LETIM0, output channel 1.
LEU0_RX		PB14		PF1	PA0			LEUART0 Receive input.
LEU0_TX		PB13		PF0	PF2			LEUART0 Transmit output. Also used as receive input in half duplex communication.
LFXTAL_N	PB8							Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin.
LFXTAL_P	PB7							Low Frequency Crystal (typically 32.768 kHz) positive pin.
PCNT0_S0IN			PC0	PD6				Pulse Counter PCNT0 input number 0.
PCNT0_S1IN	PC14		PC1	PD7				Pulse Counter PCNT0 input number 1.
TIM0_CC0	PA0	PA0			PA0	PF0		Timer 0 Capture Compare input / output channel 0.
TIM0_CC1					PC0	PF1		Timer 0 Capture Compare input / output channel 1.

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
TIM0_CC2					PC1	PF2		Timer 0 Capture Compare input / output channel 2.
TIM1_CC0				PB7	PD6			Timer 1 Capture Compare input / output channel 0.
TIM1_CC1	PC14			PB8	PD7			Timer 1 Capture Compare input / output channel 1.
TIM1_CC2	PC15	PE12		PB11				Timer 1 Capture Compare input / output channel 2.
US0_CLK	PE12			PC15	PB13	PB13		USART0 clock input / output.
US0_CS	PE13			PC14	PB14	PB14		USART0 chip select input / output.
US0_RX				PE12	PB8	PC1		USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO).
US0_TX				PE13	PB7	PC0		USART0 Asynchronous Transmit.Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI).
US1_CLK	PB7		PF0					USART1 clock input / output.
US1_CS	PB8		PF1					USART1 chip select input / output.
US1_RX	PC1		PD6					USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO).
US1_TX	PC0		PD7					USART1 Asynchronous Transmit.Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI).

4.3 GPIO pinout overview

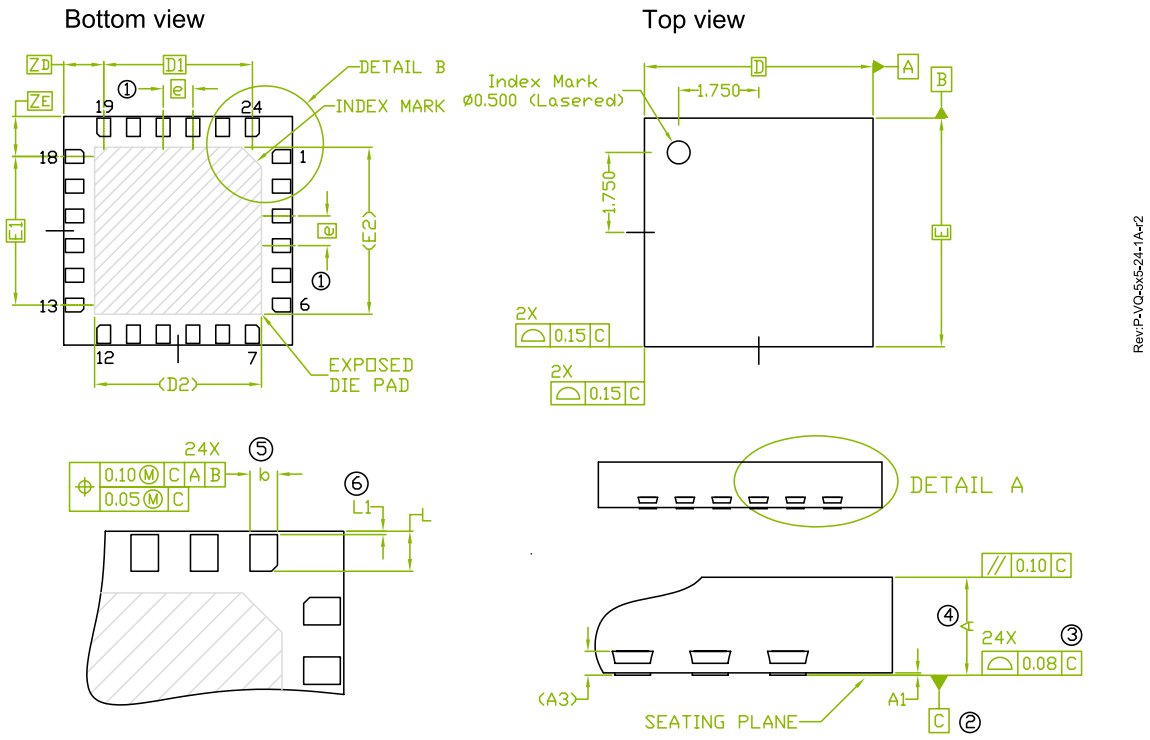
The specific GPIO pins available in *EFM32TG110* is shown in Table 4.3 (p. 40). Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port in indicated by a number from 15 down to 0.

Table 4.3. GPIO Pinout

Port	Pin 15	Pin 14	Pin 13	Pin 12	Pin 11	Pin 10	Pin 9	Pin 8	Pin 7	Pin 6	Pin 5	Pin 4	Pin 3	Pin 2	Pin 1	Pin 0
Port A	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	PA0
Port B	-	PB14	PB13	-	PB11	-	-	PB8	PB7	-	-	-	-	-	-	-
Port C	PC15	PC14	-	-	-	-	-	-	-	-	-	-	-	-	PC1	PC0
Port D	-	-	-	-	-	-	-	-	PD7	PD6	-	-	-	-	-	-
Port E	-	-	PE13	PE12	-	-	-	-	-	-	-	-	-	-	-	-
Port F	-	-	-	-	-	-	-	-	-	-	-	-	-	PF2	PF1	PF0

4.4 QFN24 Package

Figure 4.2. QFN24 (Preliminary)



Note:

1. 'e' represents the basic terminal pitch. Specifies the true geometric position of the terminal axis.
2. Datum 'C' is the mounting surface with which the package is in contact
3. Specifies the vertical shift of the flat part of each terminal form the mounting surface.
4. Dimension 'A' includes package warpage.
5. Dimension 'b' applies to metallized terminal and is measured between 0.15 mm and 0.30 mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension 'b' should not be measured in the radius area.
6. Depending on the method of lead termination at the edge of the package, a maximum 0.15 mm pull back (L1) may be present. 'L' minus 'L1' is to be equal to or greater than 0.3 mm.
7. Package dimensions take reference from JEDEC MO-220 rev. K, variations VJJ-2, except D2 and E2.

Table 4.4. QFN24 (Preliminary) (Dimensions in mm)

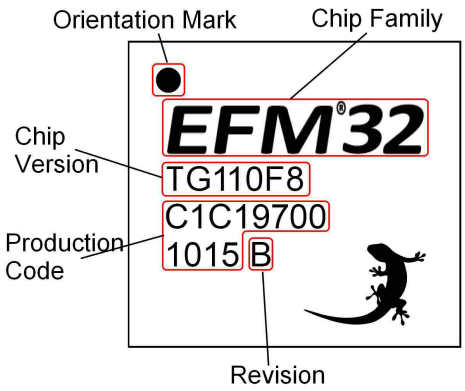
Symbol	A	A1	A3	D	D1	E	E1	e	L1	ZD	ZE	b	L	D2	E2
Min	-	0.00							0.03			0.25	0.35	3.50	3.50
Nom	0.80	0.02	0.20	5.00	3.25	5.00	3.25	0.65	-	0.875	0.875	0.30	0.40	3.65	3.65
Max	0.90	0.05							0.15			0.35	0.45	3.80	3.80

5 Chip Marking, Revision and Errata

5.1 Chip Marking

In the illustration below package fields and position are shown.

Figure 5.1. QFN24 Chip Marking



5.2 Revision

The revision of a chip can be determined from the "Revision" field in Figure 5.1 (p. 42). If the revision says "ES" (Engineering Sample), the revision must be read out electronically as speficied in the reference manual.

5.3 Errata

No known errata for the EFM32TG110.

6 Revision History

6.1 Revision 0.70

August 16th, 2010

Added pinout.

6.2 Revision 0.50

May 25th, 2010

Block diagram update.

6.3 Revision 0.40

March 26th, 2010

Initial preliminary release.

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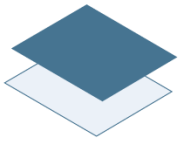

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