30 October 2002

# HFCT-5760 IBIS Model (Revision 1.0)

Agilent Technologies

# IBIS Files for Fiber-Optic Transceiver HFCT-5760
# - General Comments -

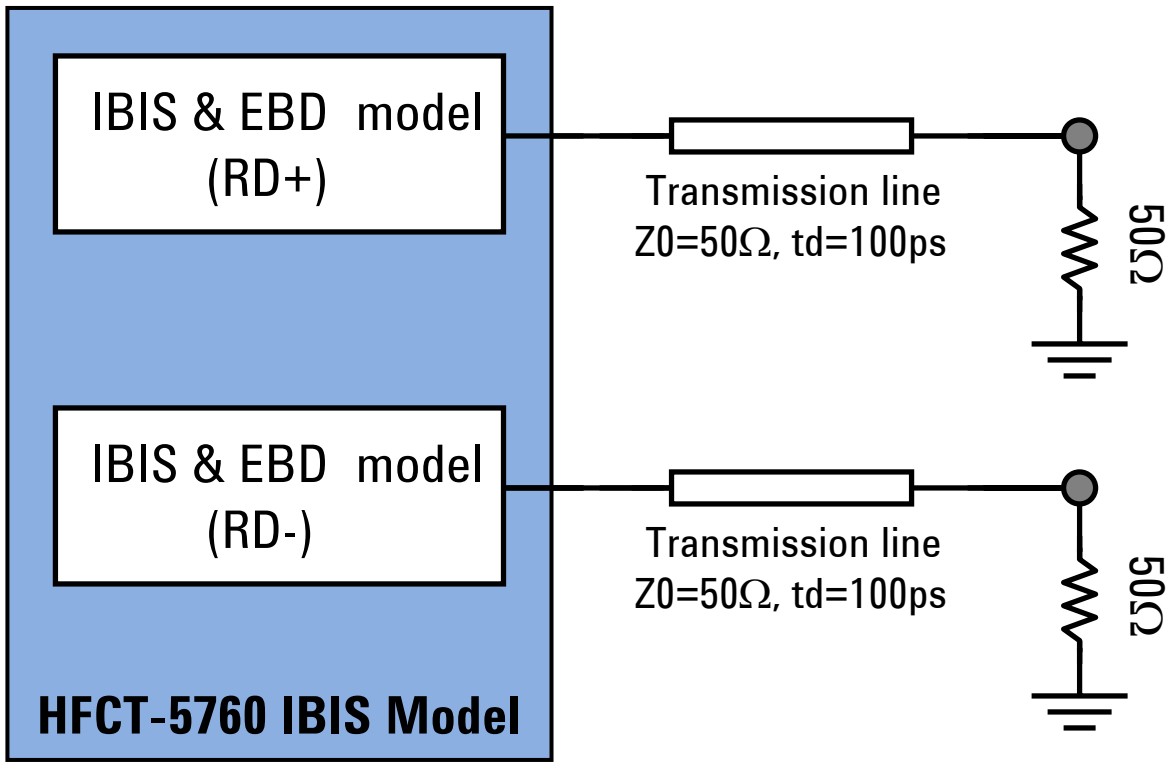
The high-speed input and output buffers of the IBIS file and the corresponding PCB path descriptions in the .ebd file have been tested by AGILENT TECHNOLOGIES with commercial EDA tools and are believed to represent an accurate description of typical component characteristics. However, the correctness of the model can not be warranted and AGILENT TECHNOLOGIES does not assume any liability arising out of the application or use of this IBIS model. Please see also the disclaimers in the IBIS model files.

AGILENT TECHNOLOGIES strives to continuously improve the quality of its IBIS models and therefore welcomes feedback on the behaviour of its models. Please address comments to the contact named on AGILENT TECHNOLOGIES' IBIS webpage. When contacting AGILENT TECHNOLOGIES, please provide the following information:

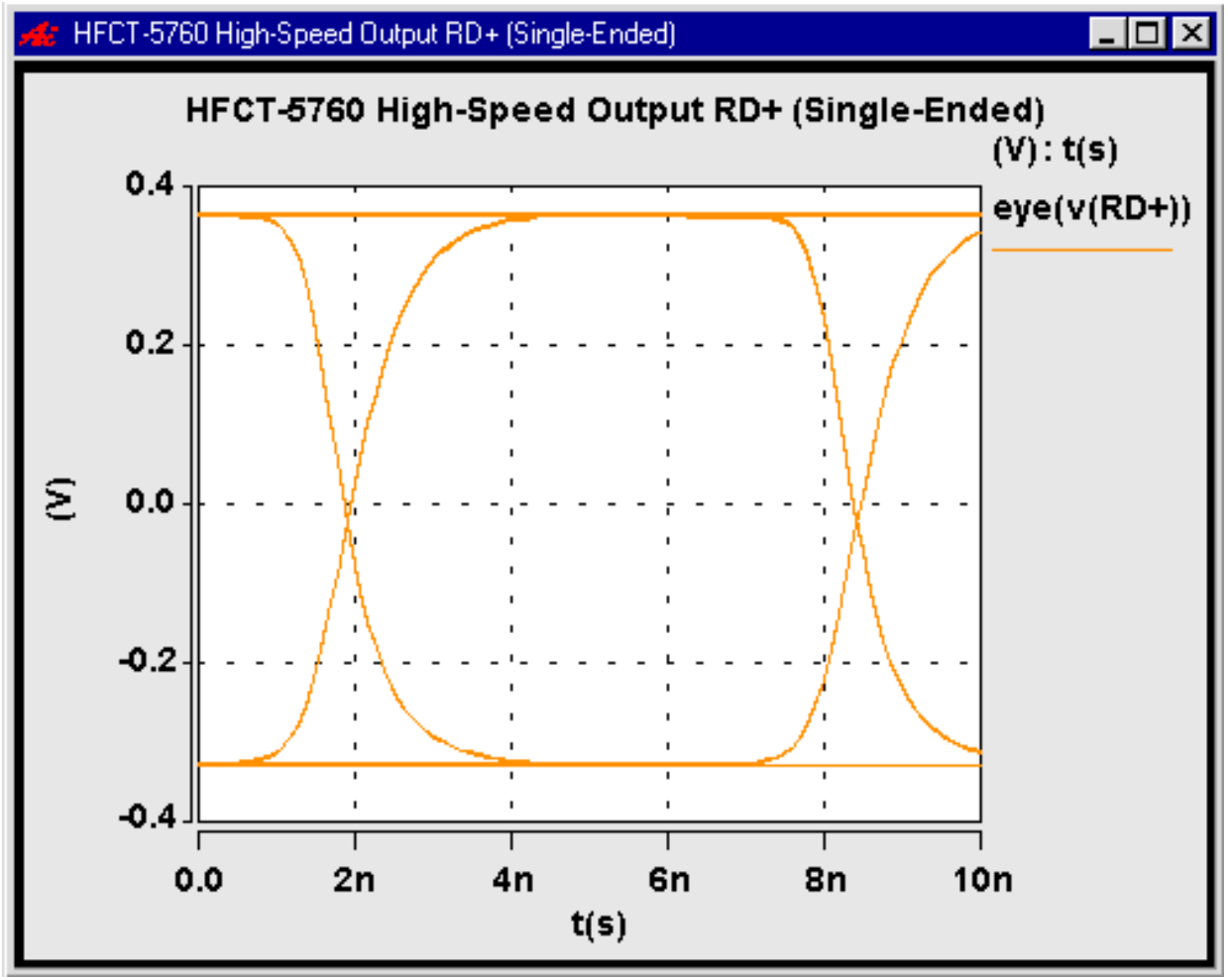
i) Component Name
ii) Application of the component / Details of simulation setup
iii) Details of the observed problem
iv) Simulation tool used

# HFCT-5760 High-Speed Output Buffer Verification

**The following single-ended test configuration was used:**

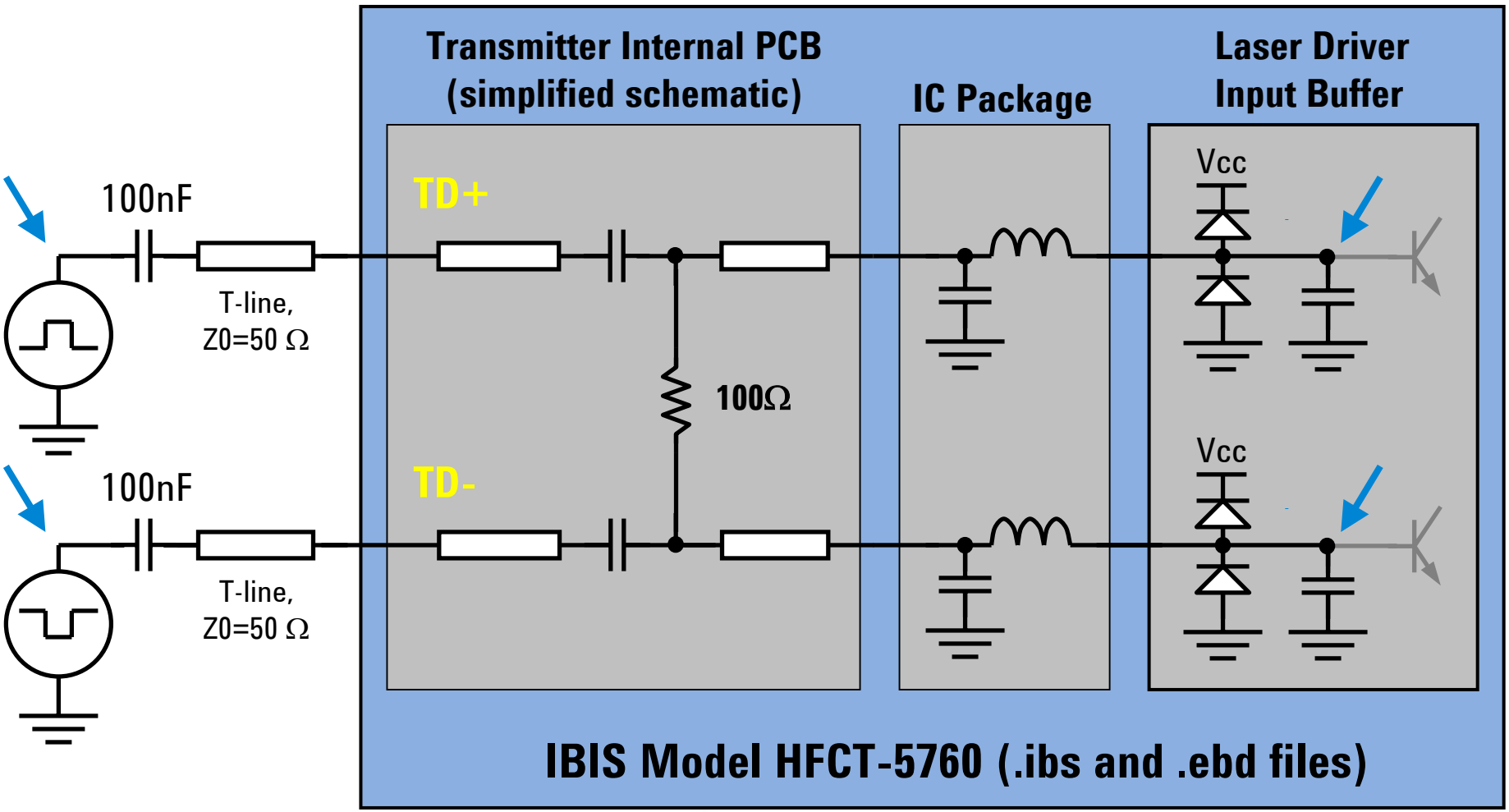


# Simulated Receiver Eye Diagram at 155MBit/s
# - Typical Data -

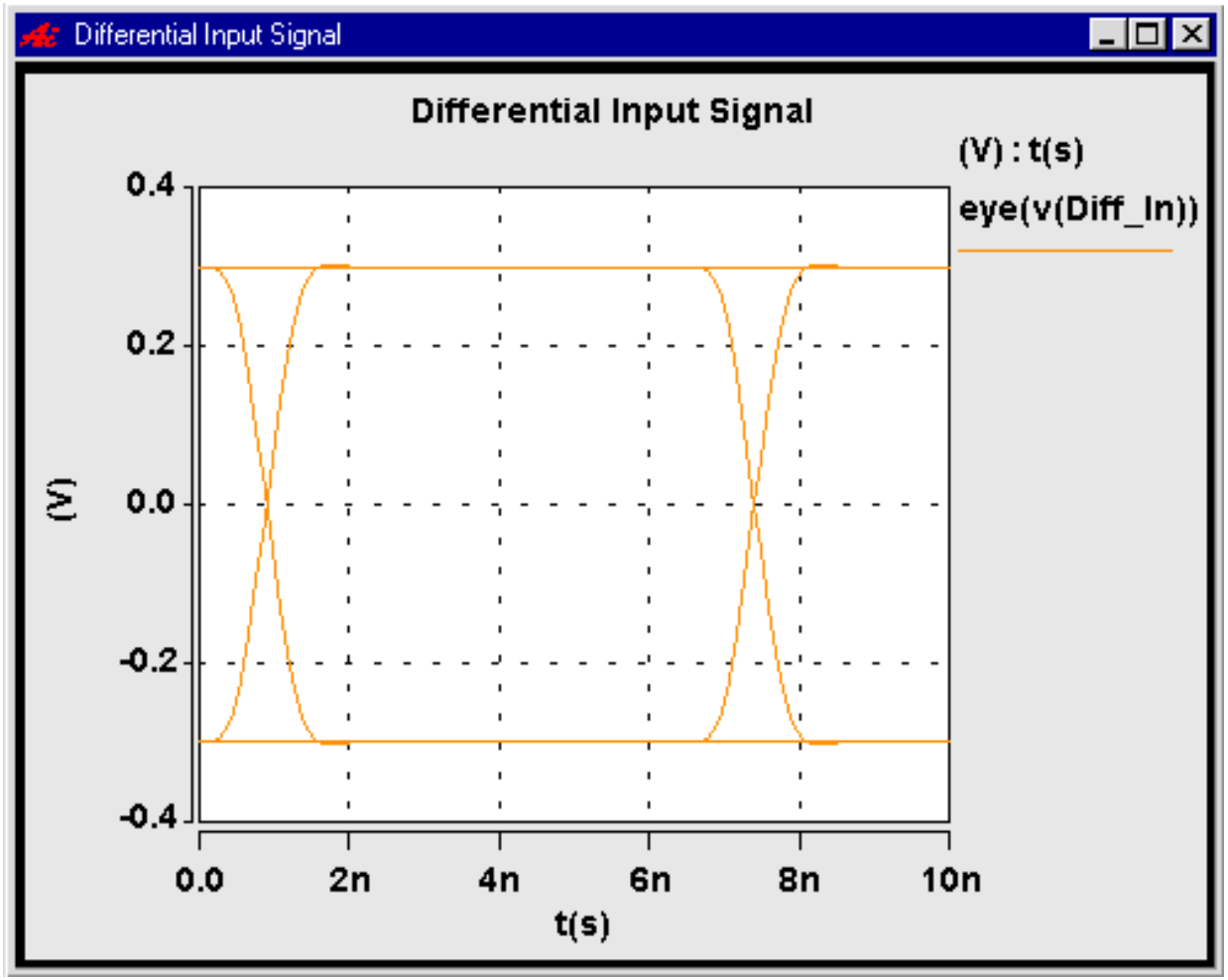


# HFCT-5760 High-Speed Input Buffers

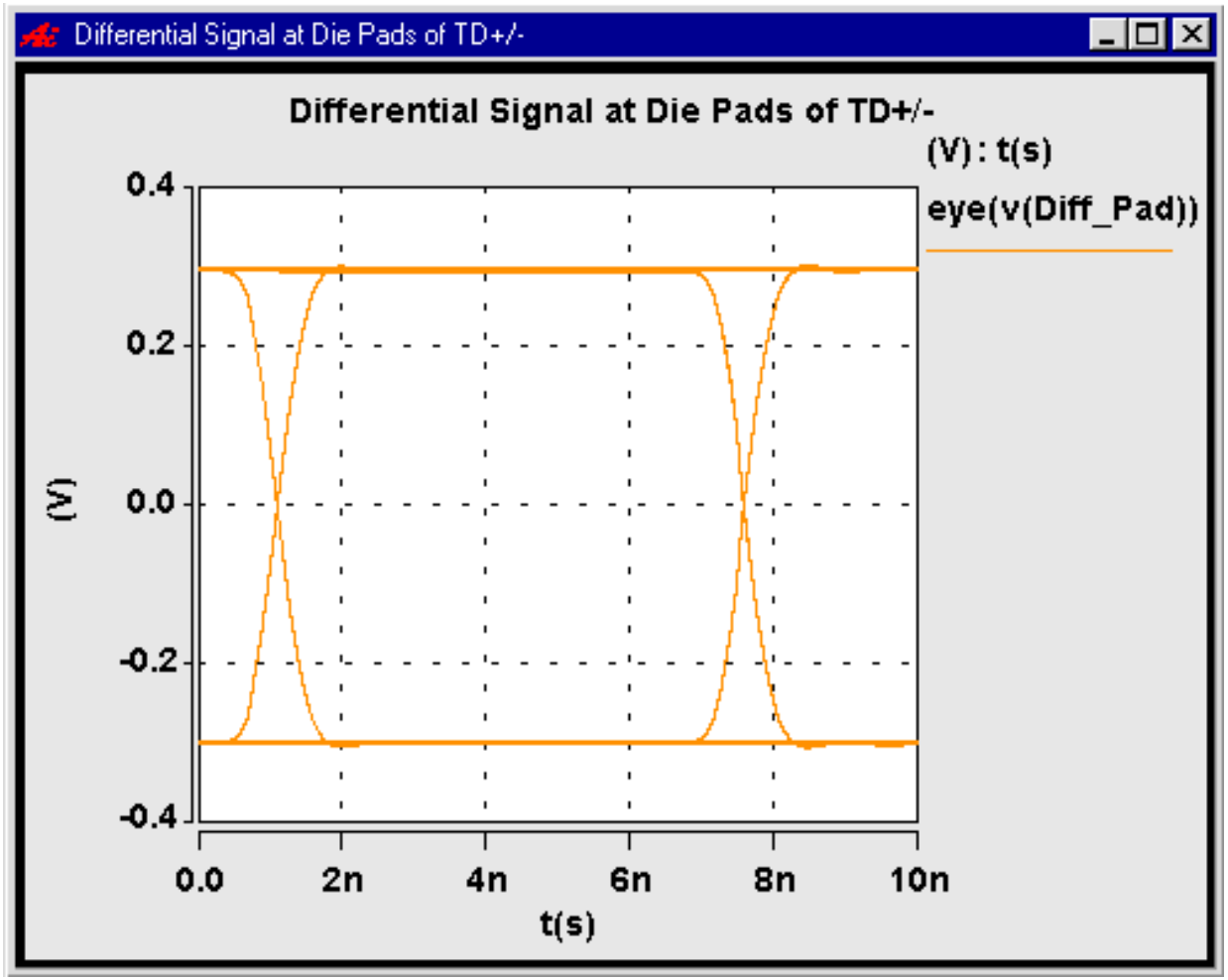
**The following test configuration was used, with the signal being probed differentially between the points that are marked by the blue arrows:**



# Input Buffer Verification – 155MBit/s Input Signal

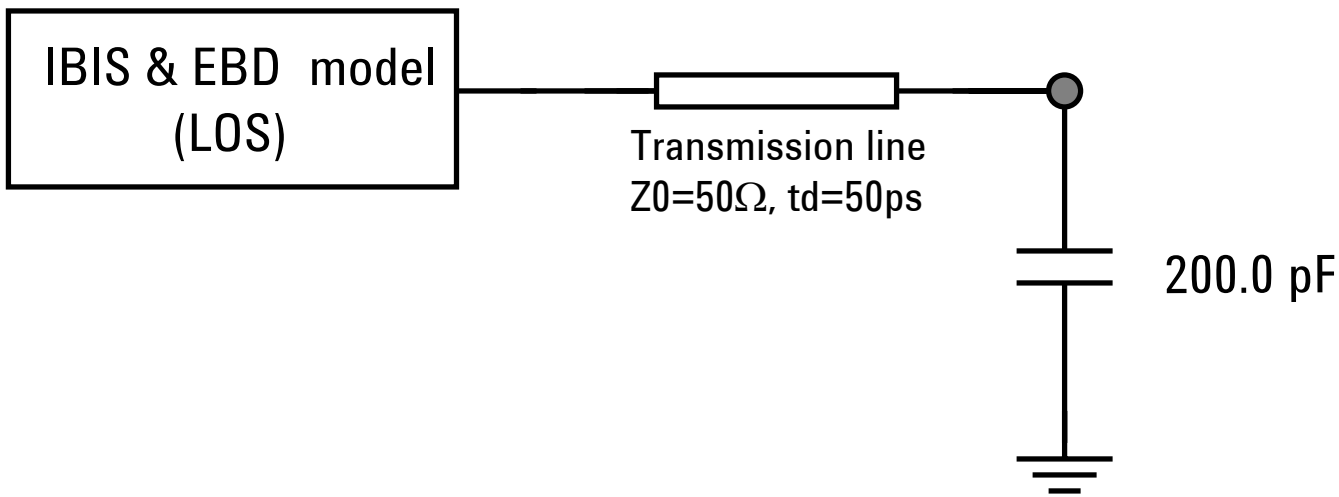


# Simulated Eye Diagram at the Die Pads
# - Typical Data -



# HFCT-5760 Loss-of-Signal (LOS) Output Buffer Verification

**The following test configuration was used:**

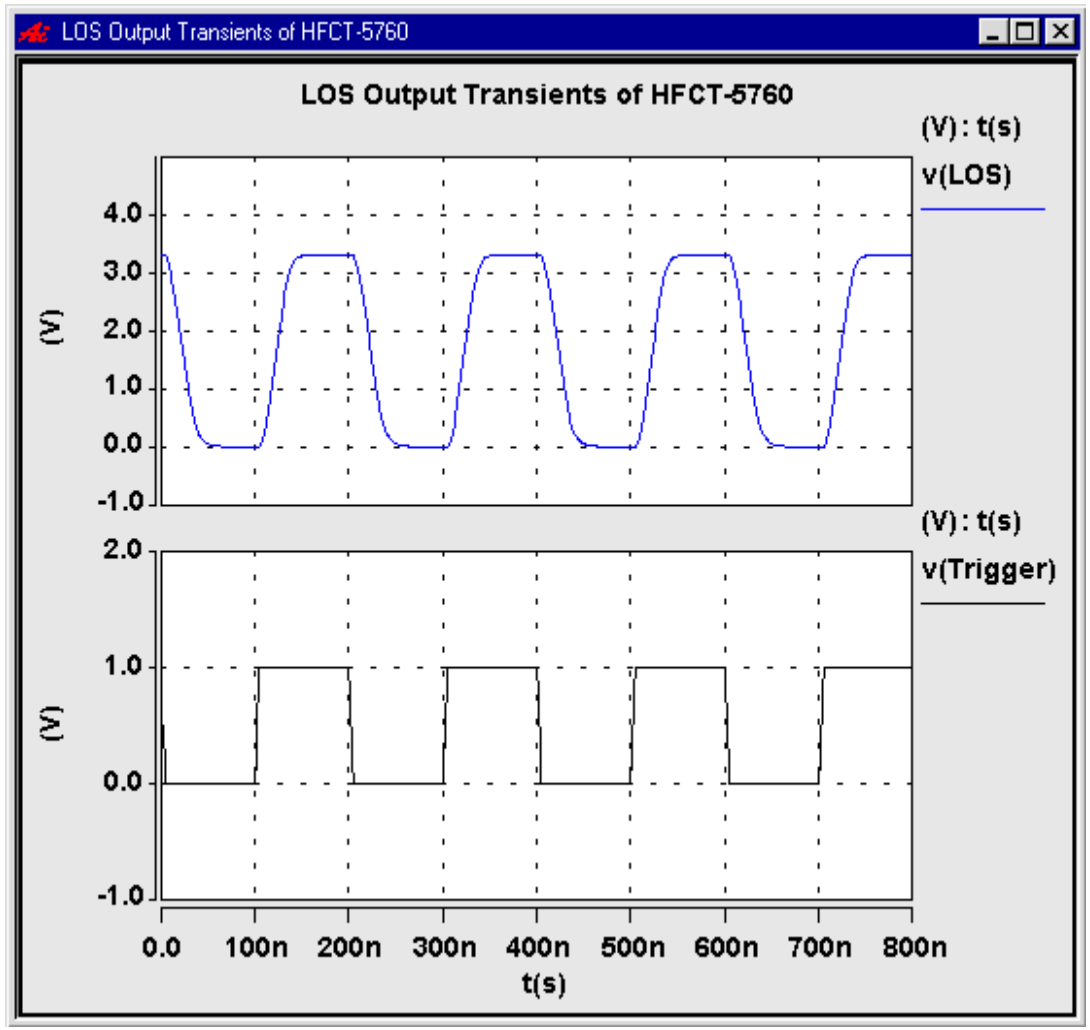


# LOS Output Transients

**This diagram shows the switching behaviour of the LOS output of transceiver HFCT_5760.**

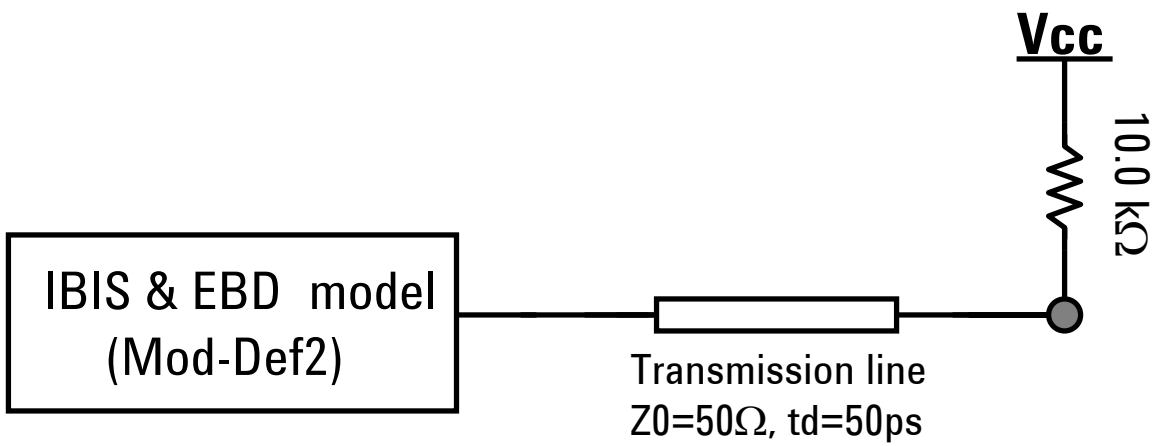
**The bottom trace shows the trigger signal that switches the buffer.**

**The top trace shows the voltage at the component pin.**



# HFCT-5760 Mod_Def2
# I/O Buffer Verification

**The following test configuration was used:**

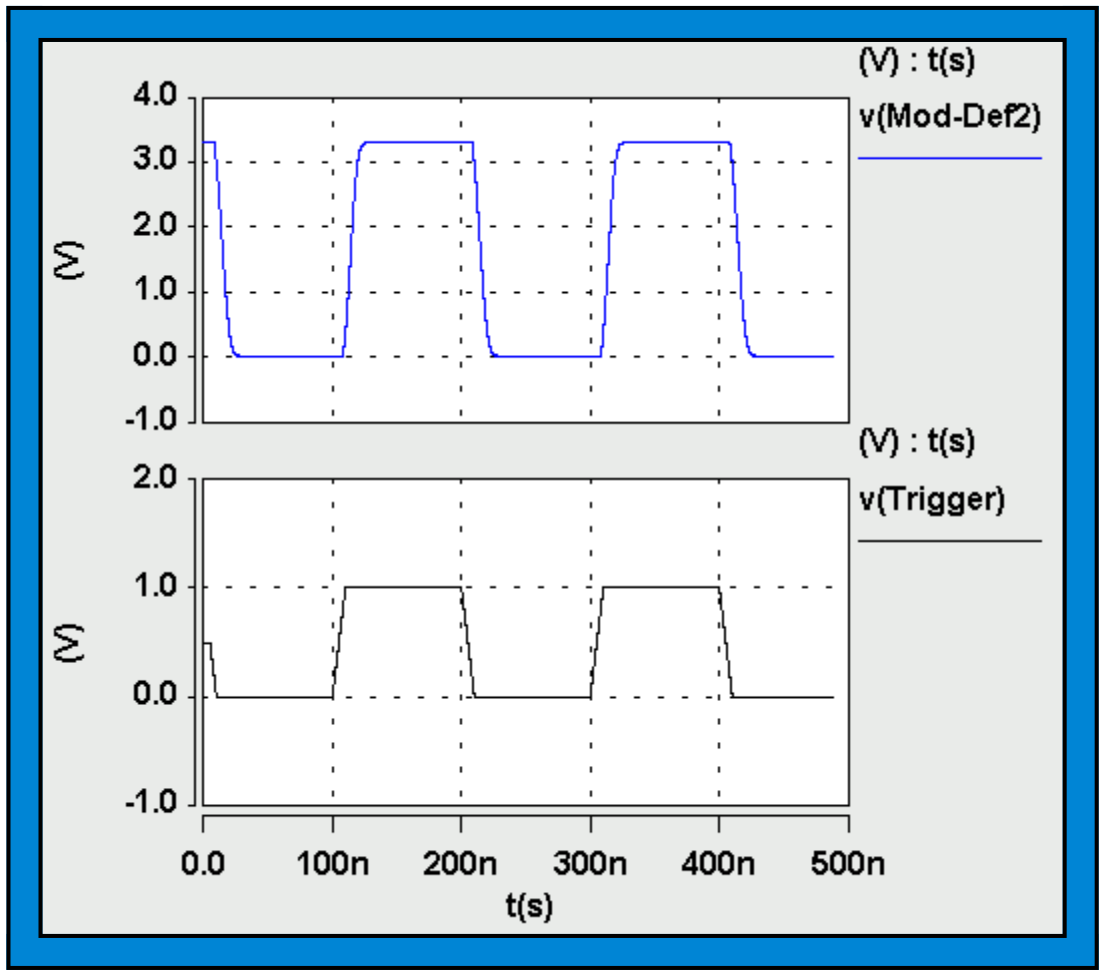


# Mod_Def2 Output Transients

**This diagram shows the switching behaviour of the Mod_Def2 output of transceiver HFCT_5760.**

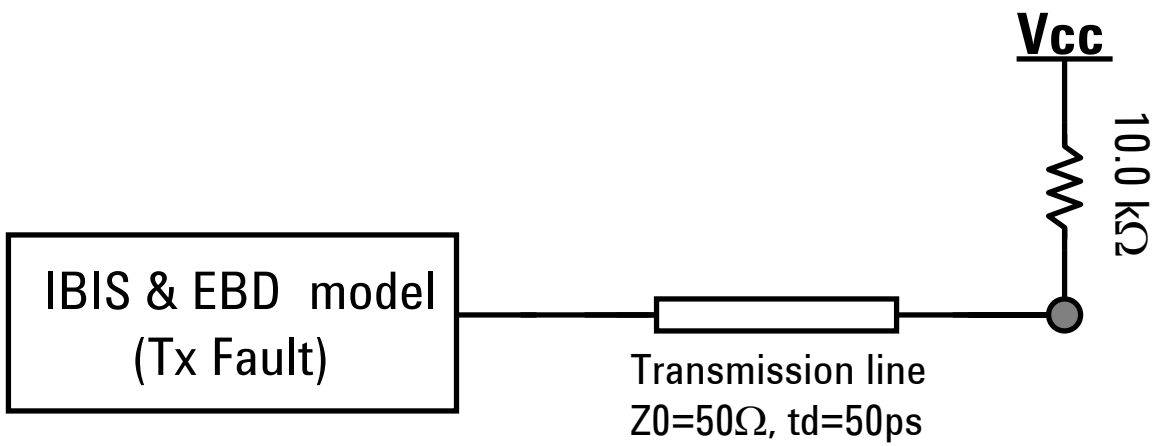
**The bottom trace shows the trigger signal that switches the buffer.**

**The top trace shows the voltage at the component pin.**



# HFCT-5760 Tx Fault
# Output Buffer Verification

**The following test configuration has been used:**



# TX Fault Output Transients

**This diagram shows the switching behaviour of the TxFault output of transceiver HFCT_5760.**

**The bottom trace shows the trigger signal that switches the buffer.**

**The top trace shows the voltage at the component pin.**