VMMK-2403

2 to 4 GHz GaAs High Linearity LNA in Wafer Level Package

Data Sheet

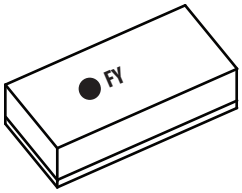
Lead (Pb) Free
RoHS 6 fully
compliant

Description

Avago's VMMK-2403 is an easy-to-use, high linearity low noise amplifier in a miniaturized wafer level package (WLP). The low noise and unconditionally stable performance makes this amplifier ideal as a primary or subsequent gain block of an RF receiver in applications from 2–4GHz. A 3V, 38mA power supply is required for optimal performance.

This amplifier is fabricated with enhancement E-pHEMT technology and industry leading revolutionary wafer level package. The GaAsCap wafer level sub-miniature leadless package is small and ultra thin yet can be handled and placed with standard 0402 pick and place assembly. This product is easy to use since it requires only positive DC voltages for bias and no matching coefficients are required for impedance matching to 50 Ω systems.

WLP 0402, 1mm x 0.5mm x 0.25 mm



Features

- 1 x 0.5 mm Surface Mount Package
- Ultrathin (0.25mm)
- Unconditionally Stable
- 50Ohm Input and Output Match
- RoHS6 + Halogen Free

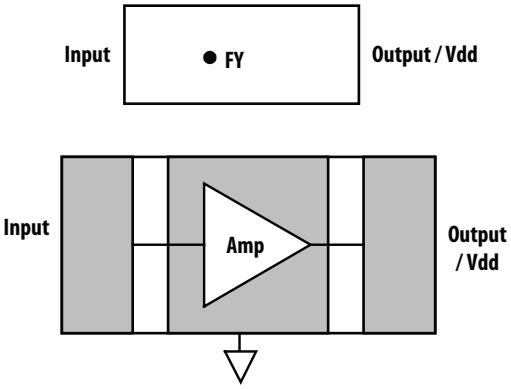
Specifications (Vdd = 3.0V, Idd = 37mA)

- Output IP3: 28dBm
- Small-Signal Gain: 16dB
- Noise Figure: 1.7dB

Applications

- 2.4 GHz, 3.5GHz WLAN and WiMax notebook computer, access point and mobile wireless applications
- 802.16 & 802.20 BWA systems
- Radar, radio and ECM systems

Pin Connections (Top View)



Note:
"F" = Device Code
"Y" = Month Code

Attention: Observe precautions for handling electrostatic sensitive devices.
ESD Machine Model (Class A)
ESD Human Body Model (Class 1A)
Refer to Avago Application Note A004R: Electrostatic Discharge, Damage and Control.

Table 1. Absolute Maximum Ratings

Sym	Parameters/Condition	Unit	Absolute Max
Vd	Supply Voltage (RF Output) [2]	V	10
Id	Device Current [2]	mA	70 mA
$P_{in, max}$	CW RF Input Power (RF Input) [3]	dBm	+20 dBm
P_{diss}	Total Power Dissipation	mW	300 mW
Tch	Max channel temperature	°C	+150
T_{STG}	Storage Temperature	°C	+150
θjc	Thermal Resistance [4]	°C/W	160

Notes
1. Operation of this device above any one of these parameters may cause permanent damage
2. Bias is assumed DC quiescent conditions
3. With the DC (typical bias) and RF applied to the device at board temperature Tb = 25°C
4. Thermal resistance is measured from junction to board using IR method

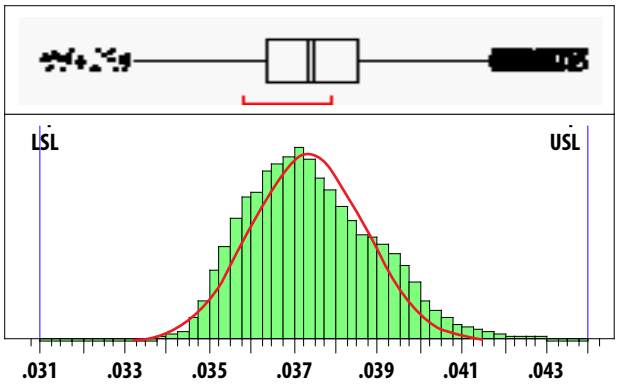
Table 2. DC and RF Specifications

T_A = 25°C, Frequency = 3 GHz, Vd = 3V, I_d = 38mA, $Z_{in} = Z_{out}$ = 50Ω (unless otherwise specified)

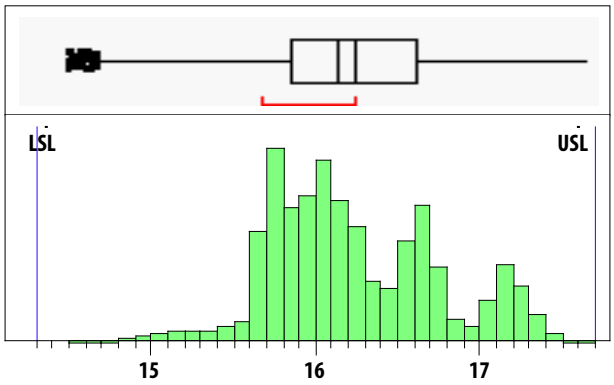
Sym	Parameters/Condition	Unit	Minimum	Typ.	Maximum
Id	Device Current	mA	30	37	45
NF [1,2]	Noise Figure	dB	–	1.7	2.2
Ga [1,2]	Associated Gain	dB	14	16	17
OIP3 [1,2,3]	Output 3rd Order Intercept	dBm	+26	+27.8	–
P-1dB[1,2]	Output Power at 1dB Gain Compression	dBm		+16.5	–
IRL [1,2]	Input Return Loss	dB	–	-12	–
ORL [1,2]	Output Return Loss	dB	–	-12	–

Notes:
1. Losses of test systems have been de-embedded from final data
2. Measure Data obtained from wafer-probing
3. OIP3 test condition: F1=3.0GHz, F2=3.01GHz, Pin=-20dBm

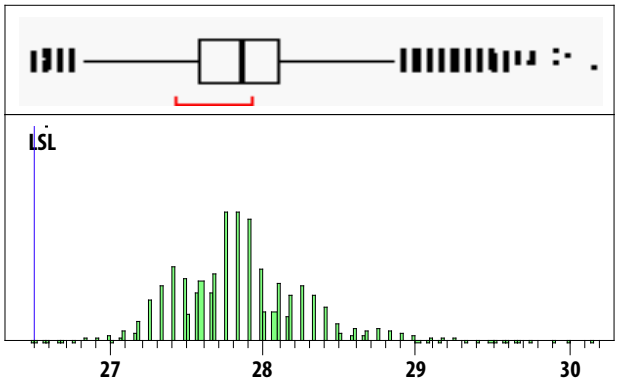
Product Consistency Distribution Charts at 3.0 GHz, Vd = 3V



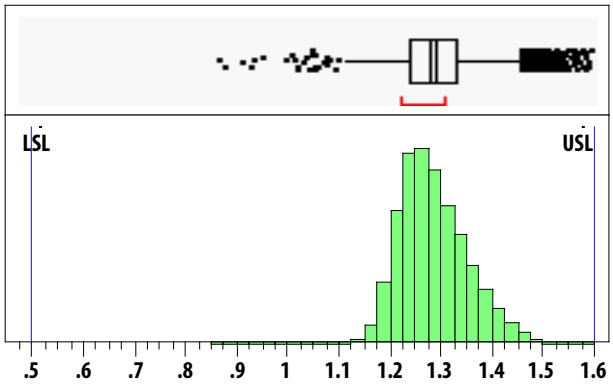
Id, LSL=0.030 A, Nominal=0.037 A, USL=0.045 A



Gain @ 3GHz, LSL=14 dB, Nominal=16 dB, USL=18 dB



OIP3 at 3GHz, LSL=26 dBm, Nominal=27.85 dBm



NF @ 3GHz, Nominal=1.69 dB, USL=2.20 dB

Note: Distribution data based on 500 part sample size from skew lots during initial characterization.

VMMK-2403 Typical Performance

(T_A = 25°C, Vdd = 3V, Idd = 38mA, Z_{in} = Z_{out} = 50 Ω unless noted)

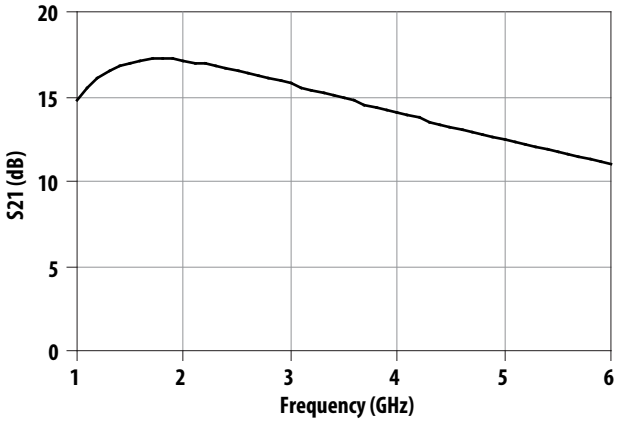


Figure 1. Small-signal Gain [1]

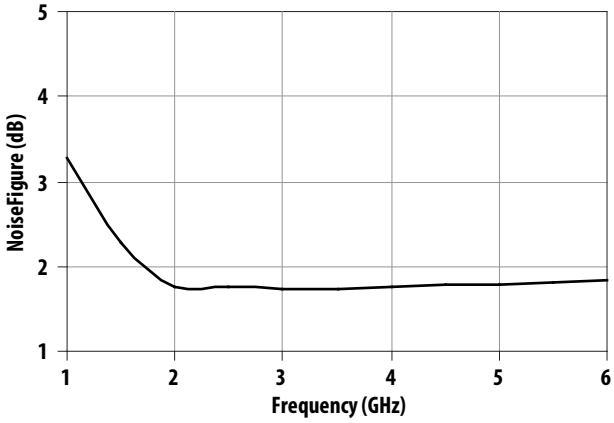


Figure 2. Noise Figure [1]

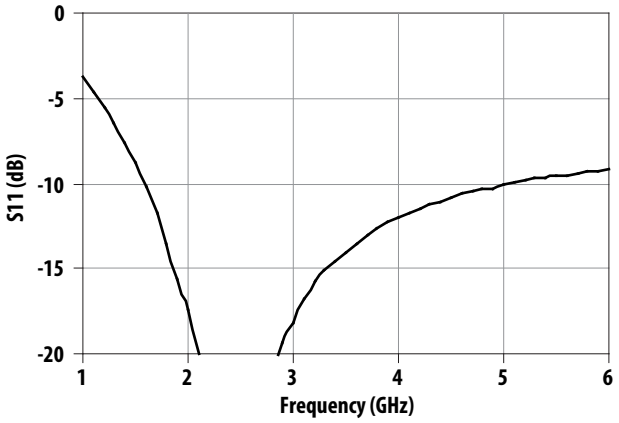


Figure 3. Input Return Loss [1]

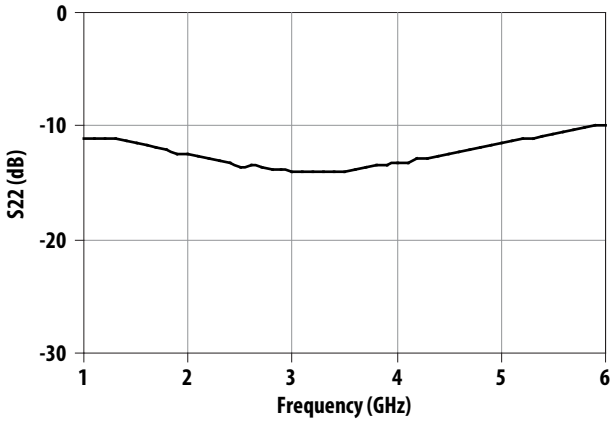


Figure 4. Output Return Loss [1]

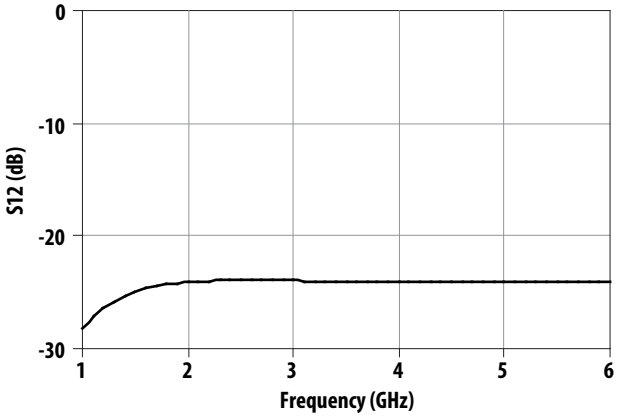


Figure 5. Isolation [1]

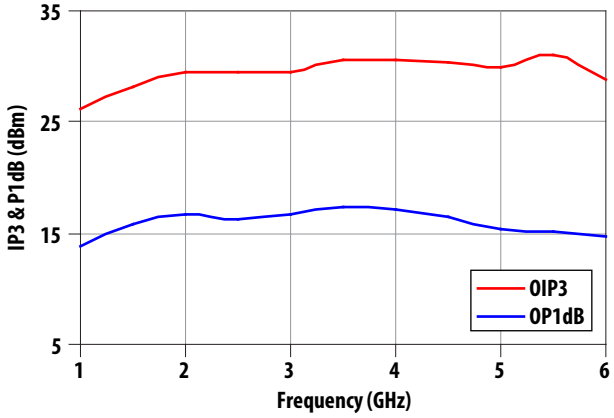


Figure 6. Output IP3 & Output P1dB [1,2]

Notes:
1. Data taken on a G-S-G probe substrate fully de-embedded to the reference plane of the package
2. Output IP3 data taken at Pin=-15dBm

VMMK-2403 Typical Performance (continue)

(T_A = 25°C, Vdd = 3V, Idd = 38mA, Z_{in} = Z_{out} = 50 Ω unless noted)

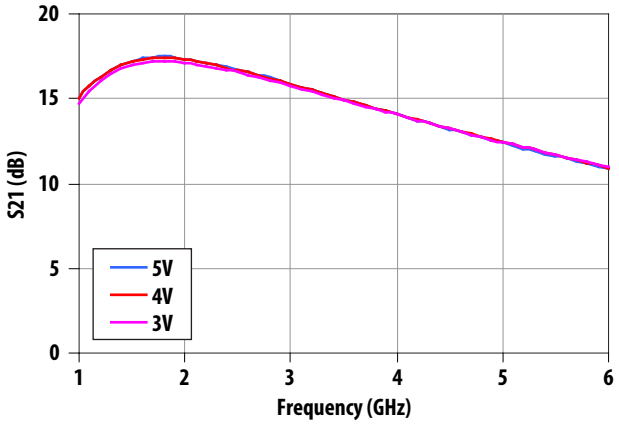


Figure 7. Gain over Vdd [1]

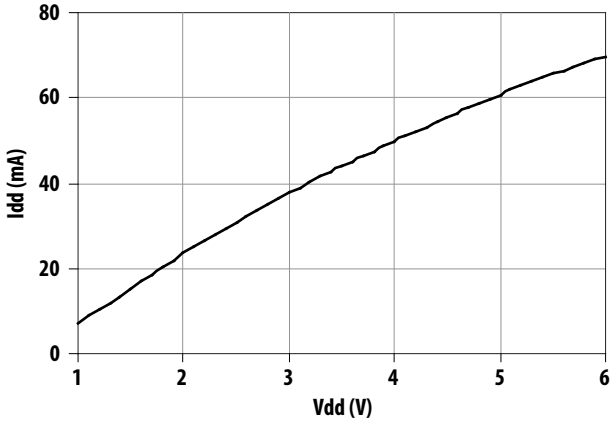


Figure 8. Total Current [1]

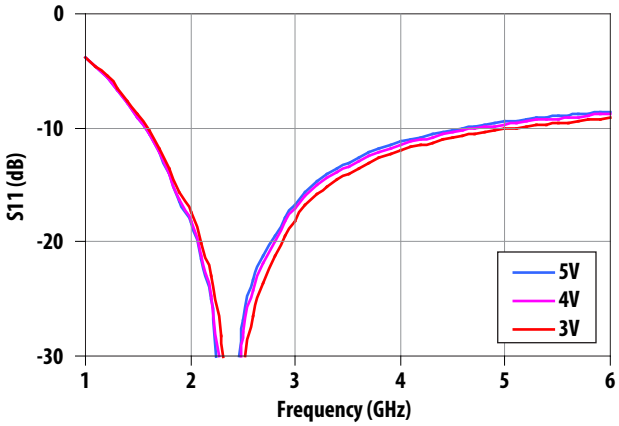


Figure 9. Input Return Loss over Vdd [1]

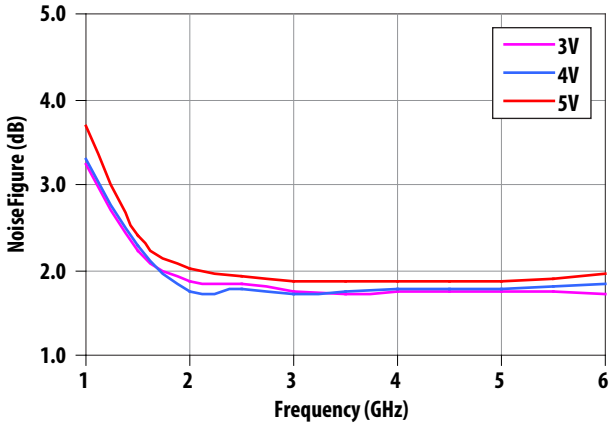


Figure 10 Noise Figure over Vdd [1]

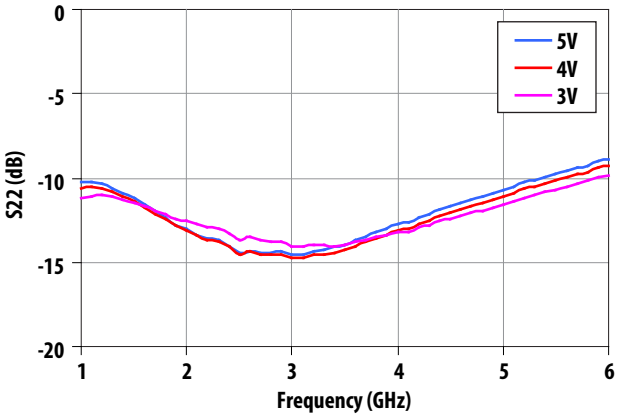


Figure 11. Output Return Loss Over Vdd [1]

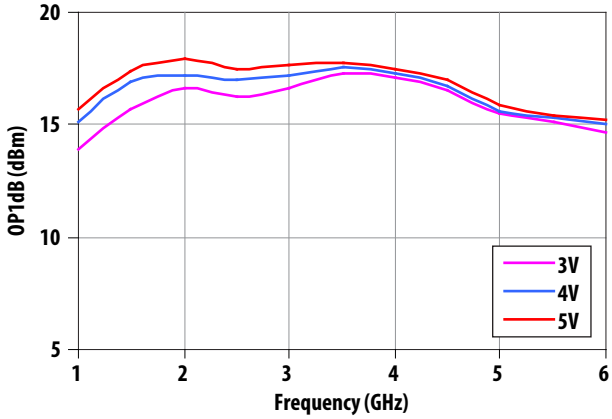


Figure 12. Output P1dB Over Vdd [1]

Notes:

1. Data taken on a G-S-G probe substrate fully de-embedded to the reference plane of the package

VMMK-2403 Typical Performance (continue)

(T_A = 25°C, Vdd = 3V, Idd = 38mA, Z_{in} = Z_{out} = 50 Ω unless noted)

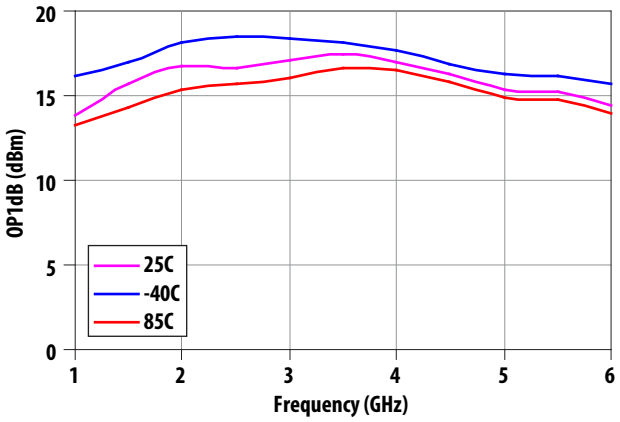


Figure 13. Output P-1dB over Temp [3]

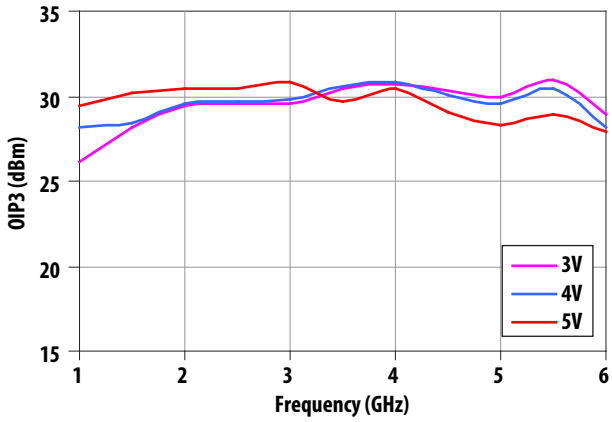


Figure 14. Output IP3 Over Vdd [2,3]

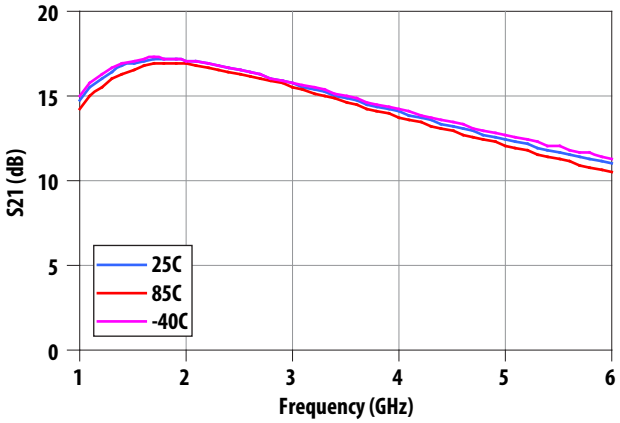


Figure 15. Gain over Temp [3]

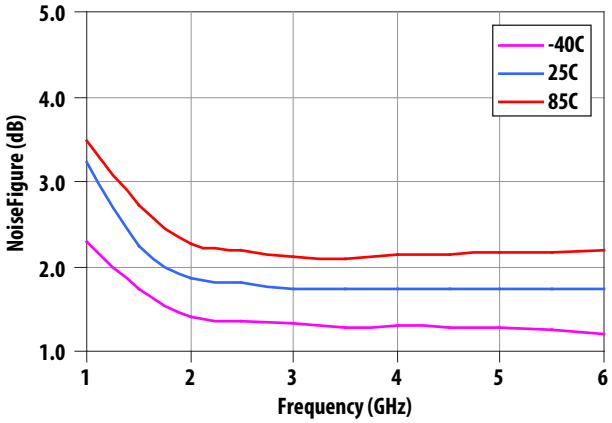


Figure 16 Noise Figure over Temp [3]

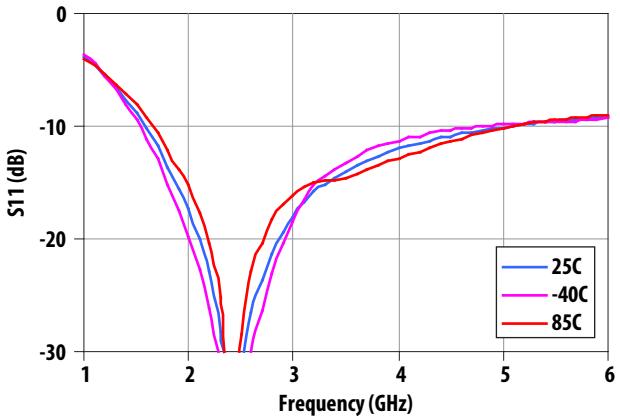


Figure 17. Input Return Loss Over Temp [3]

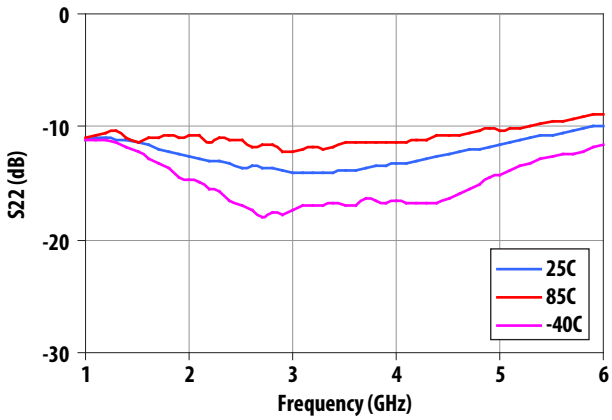


Figure 18. Output Return Loss Over Temp [3]

Notes:
1. Data taken on a G-S-G probe substrate fully de-embedded to the reference plane of the package
2. Output IP3 data taken at Pin=-15dBm
3. Over temp data taken on a test fixture (Figure 20) without de-embedding

VMMK-2403 Typical S-parameters

T_A = 25°C, Vdd = 3V, Idd = 38mA, Z_{in} = Z_{out} = 50 Ω unless noted)

Freq	S11			S21			S12			S22		
GHz	Mag	dB	Phase	Mag	dB	Phase	Mag	dB	Phase	Mag	dB	Phase
1	0.65	-3.79	113.52	5.47	14.76	-144.36	0.04	-28.13	87.94	0.28	-11.18	-10.64
1.5	0.36	-8.82	81.05	7.05	16.97	-178.05	0.05	-24.97	60.57	0.27	-11.46	-58.54
2.0	0.13	-17.40	55.74	7.16	17.09	155.06	0.06	-24.10	42.05	0.24	-12.53	-87.61
2.5	0.03	-31.80	-133.91	6.71	16.53	134.46	0.06	-23.90	30.73	0.21	-13.69	-100.64
3.0	0.12	-18.13	-151.55	6.12	15.74	117.90	0.06	-23.97	23.43	0.20	-14.03	-105.66
3.5	0.20	-14.05	-163.87	5.55	14.88	104.00	0.06	-24.04	19.19	0.20	-13.96	-107.15
4.0	0.25	-12.00	-174.32	5.04	14.05	91.92	0.06	-24.14	15.78	0.22	-13.22	-106.91
4.5	0.29	-10.89	175.98	4.58	13.22	81.08	0.06	-24.14	13.35	0.24	-12.42	-108.59
5.0	0.31	-10.13	167.30	4.19	12.44	71.14	0.06	-24.12	12.04	0.26	-11.58	-110.59
5.5	0.33	-9.59	159.43	3.84	11.69	61.94	0.06	-24.07	10.81	0.29	-10.73	-113.90
6.0	0.35	-9.16	151.41	3.54	10.97	53.04	0.06	-24.01	9.65	0.32	-9.87	-118.40
6.5	0.36	-8.91	143.69	3.26	10.27	44.57	0.06	-23.89	8.81	0.35	-9.03	-123.20
7.0	0.37	-8.69	136.41	3.02	9.59	36.31	0.07	-23.74	8.13	0.39	-8.27	-128.23
7.5	0.38	-8.50	129.27	2.79	8.91	28.19	0.07	-23.58	7.21	0.42	-7.52	-133.56
8.0	0.38	-8.36	122.37	2.58	8.25	20.21	0.07	-23.39	6.48	0.46	-6.81	-139.38
8.5	0.39	-8.21	115.19	2.39	7.56	12.37	0.07	-23.22	5.74	0.49	-6.17	-144.98
9.0	0.39	-8.12	108.46	2.20	6.85	4.43	0.07	-23.06	4.98	0.53	-5.53	-151.26
9.5	0.40	-7.98	101.84	2.02	6.11	-3.50	0.07	-22.83	4.19	0.56	-4.98	-158.01
10.0	0.41	-7.83	95.04	1.84	5.30	-11.35	0.07	-22.60	3.57	0.60	-4.39	-164.68
10.5	0.41	-7.72	88.39	1.66	4.40	-19.19	0.08	-22.34	2.72	0.64	-3.88	-172.30
11.0	0.42	-7.59	82.22	1.48	3.39	-26.92	0.08	-22.09	2.06	0.67	-3.42	179.91
11.5	0.43	-7.42	76.20	1.29	2.22	-34.30	0.08	-21.79	1.40	0.71	-2.99	171.62
12.0	0.43	-7.25	70.01	1.10	0.82	-41.13	0.08	-21.46	0.40	0.74	-2.67	162.75

VMMK-2403 Application and Usage

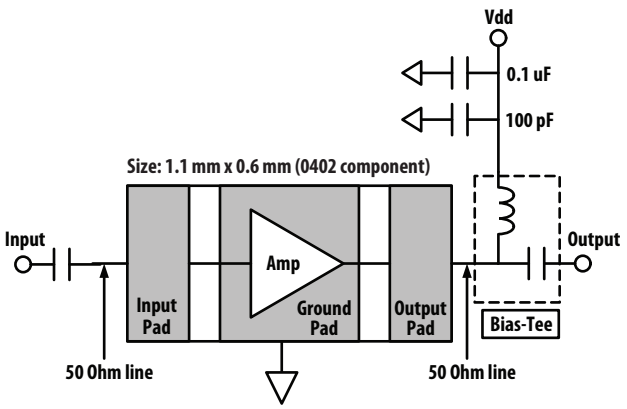


Figure 19. Usage of the VMMK-2403

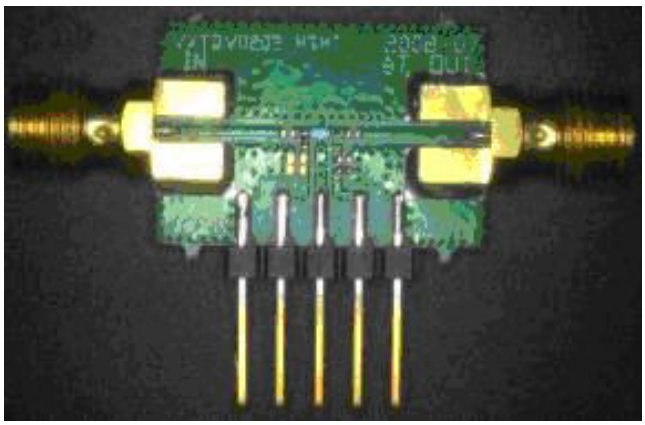


Figure 20. Evaluation/Test Board (available to qualified customer request)

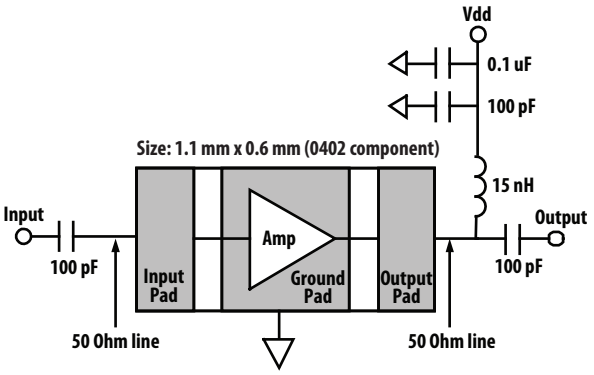


Figure 21. Example application of VMMK-2403 at 3.5GHz

Biasing and Operation

The VMMK-2403 is normally biased with a positive drain supply connected to the output pin through an external bias-tee and with bypass capacitors as shown in Figure 19. The recommended drain supply voltage is 3 V and the corresponding drain current is approximately 38mA. Aspects of the amplifier performance may be improved over a narrower bandwidth by application of additional conjugate, linearity, or low noise (τopt) matching.

Biasing the device at 3V results in slightly lower noise figure. In a typical application, the bias-tee can be constructed using lumped elements. The value of the output inductor can have a major effect on both low and high frequency operation. The demo board uses a 15 nH inductor which provides an optimum value for 2 to 4 GH operation. If operation is desired at frequencies higher than 4 GHz then a smaller value such as 8.2 nH may be required to keep the self resonant frequency higher than the maximum desired frequency of operation.

Another approach for broadbanding the VMMK-2403 is to series two different value inductors with the smaller value inductor placed closest to the device and favoring the higher frequencies. The larger value inductor will then offer better low frequency performance by not loading the output of the device. The parallel combination of the 100pF and 0.1uF capacitors provide a low impedance in the band of operation and at lower frequencies and should be placed as close as possible to the inductor. The low frequency bypass provides good rejection of power supply noise and also provides a low impedance termination for third order low frequency mixing products that will be generated when multiple in-band signals are injected into any amplifier.

Refer the Absolute Maximum Ratings table for allowed DC and thermal conditions.

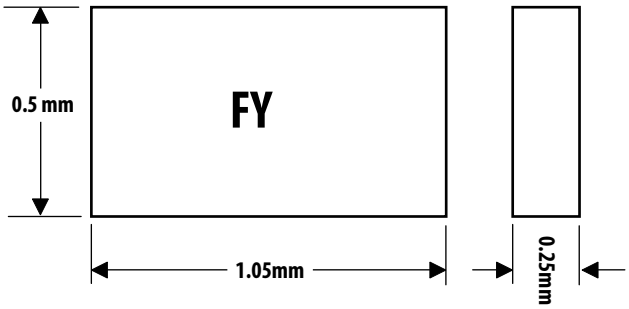
S Parameter Measurements

The S parameters are measured on a 300um G-S-G (ground signal ground) printed circuit board substrate. Calibration is achieved with a series of through, short and open substrates from which an accurate set of S parameters is created. The test board is .016 inch thickness RO4350. Grounding of the device is achieved with a single plated through hole directly under the device. The effect of this plated through hole is included in the S parameter measurements and is difficult to de-embed accurately. Since the maximum recommended printed circuit board thickness is nominally .020 inch, then the nominal effect of printed circuit board grounding can be considered to have already been included the published S parameters.

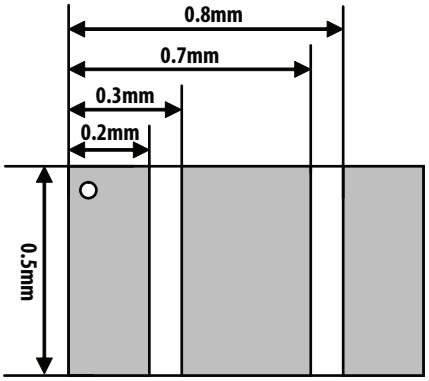
The product consistency distribution charts shown on page 2 represent data taken by the production wafer probe station using a 300um G-S wafer probe. The ground-signal probing that is used in production allows the device to be probed directly at the device with minimal common lead inductance to ground. Therefore there will be a slight difference in the nominal gain obtained at the test frequency using the 300um G-S wafer probe versus the 300um G-S-G printed circuit board substrate method.

Outline Drawing

Top and Side View

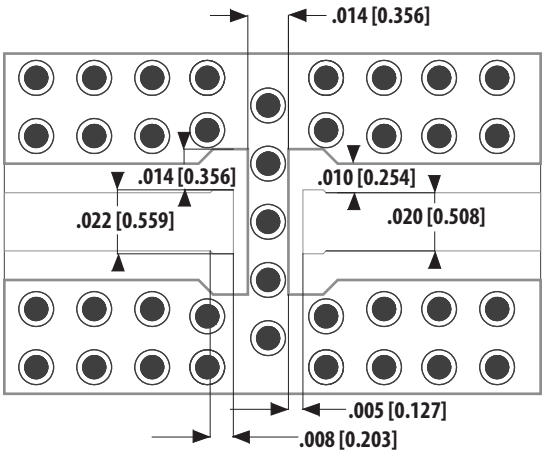


Bottom View



Notes:
1. • indicates pin 1
2. Dimensions are in millimeters
3. Pad Material is minimum 5.0 um thick Au

Suggested PCB Material and Land Pattern



Notes:
1. 0.010" Rogers RO4350

Recommended SMT Attachment

The VMMK Packaged Devices are compatible with high volume surface mount PCB assembly processes.

Manual Assembly for Prototypes

1. Follow ESD precautions while handling packages.
2. Handling should be along the edges with tweezers or from topside if using a vacuum collet.
3. Recommended attachment is solder paste. Please see recommended solder reflow profile. Conductive epoxy is not recommended. Hand soldering is not recommended.
4. Apply solder paste using either a stencil printer or dot placement. The volume of solder paste will be dependent on PCB and component layout and should be controlled to ensure consistent mechanical and electrical performance. **Excessive solder will degrade RF performance.**
5. Follow solder paste and vendor's recommendations when developing a solder reflow profile. A standard profile will have a steady ramp up from room temperature to the pre-heat temp to avoid damage due to thermal shock.
6. Packages have been qualified to withstand a peak temperature of 280°C for 15 sec. Verify that the profile will not expose device beyond these limits.
7. Clean off flux per vendor's recommendations.
8. Clean the module with Acetone. Rinse with alcohol. Allow the module to dry before testing.

Note: These devices are ESD sensitive. The following precautions are strongly recommended. Ensure that an ESD approved carrier is used when die are transported from one destination to another. Personal grounding is to be worn at all times when handling these devices. For more detail, refer to Avago Application Note A004R: Electrostatic Discharge Damage and Control

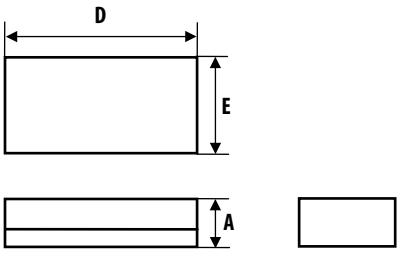
ESD Machine Model (Class A)

ESD Human Body Model (Class A)

Ordering Information

Part Number	Devices Per Container	Container
VMMK-2403-BLKG	100	Antistatic Bag
VMMK-2403-TR1G	5000	7″ Reel

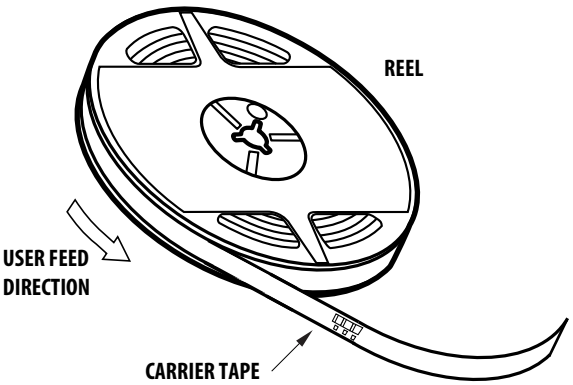
Package Dimension Outline



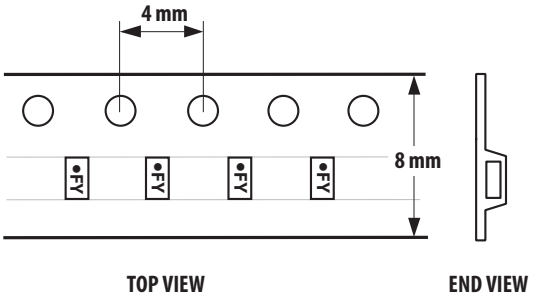
Symbol	Min (mm)	Max (mm)
E	0.500	0.566
D	1.004	1.066
A	0.235	0.265

Note:
All dimensions are in mm

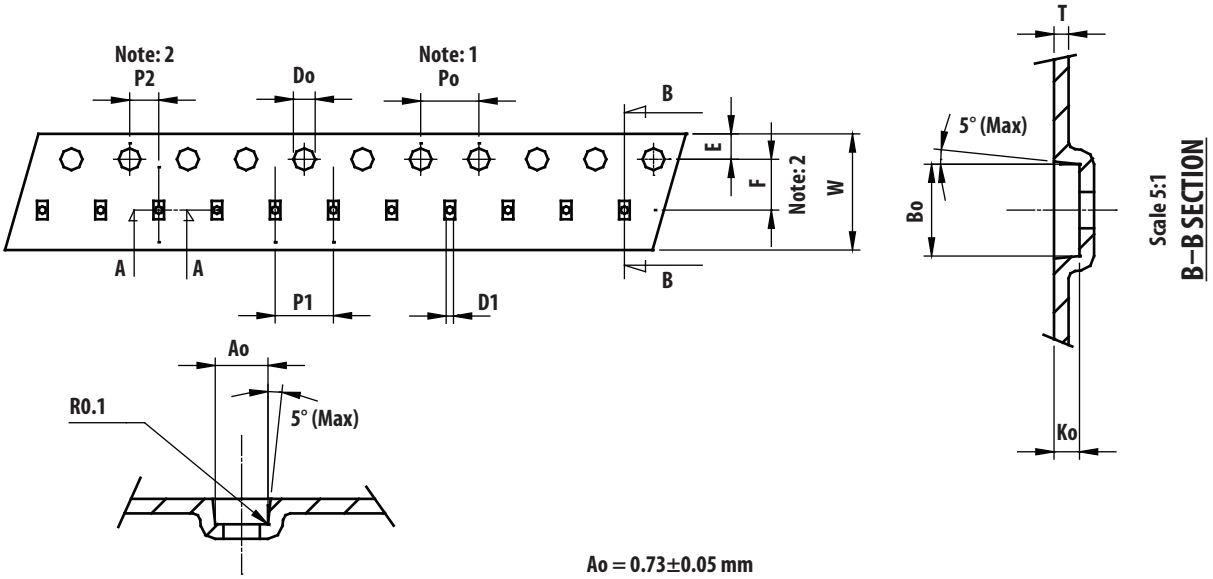
Reel Orientation



Device Orientation



Tape Dimensions



Scale 5:1

A–A SECTION

Ao = 0.73±0.05 mm

Bo = 1.26±0.05 mm

Ko = 0.35 $^{+0.05}_{+0}$ mm

Unit: mm

Symbol	Spec.
K1	–
Po	4.0±0.10
P1	4.0±0.10
P2	2.0±0.05
Do	1.55±0.05
D1	0.5±0.05
E	1.75±0.10
F	3.50±0.05
10Po	40.0±0.10
W	8.0±0.20
T	0.20±0.02

Notice:
1. 10 Sprocket hole pitch cumulative tolerance is ±0.1mm.
2. Pocket position relative to sprocket hole measured as true position of pocket not pocket hole.
3. Ao & Bo measured on a place 0.3mm above the bottom of the pocket to top surface of the carrier.
4. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
5. Carrier camber shall be not than 1m per 100mm through a length of 250mm.

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

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