Octal, 16-Bit, Low-Power, ±15-V Output, Serial Input DIGITAL-TO-ANALOG CONVERTER

FEATURES

- **Bipolar Output: ±15 V, Up to ±16.5 V**
- **Unipolar Output: 0 V to +18 V**
- **16-Bit Resolution**
- **Low Power: 20.6 mW/Ch**
- **Relative Accuracy: 4 LSB Max**
- **Low Zero-Code/Gain Error**
  - **Before User Calibration: ±10 LSB Max**
  - **After User Calibration: ±1 LSB Max**
- **Flexible System Calibration**
- **Low Glitch**
- **Settling Time: 10 μs**
- **Channel Monitor Output**
- **Programmable Offset**
- **SPI™: Up to 50-MHz, 1.8-V/3-V/5-V Logic**
- **Schmitt Trigger Inputs**
- **Daisy-Chain Mode**
- **Packages: QFN-48 (7x7mm), TQFP-64 (10x10mm)**

APPLICATIONS

- **Automatic Test Equipment**
- **PLC and Industrial Process Control**
- **Communications**

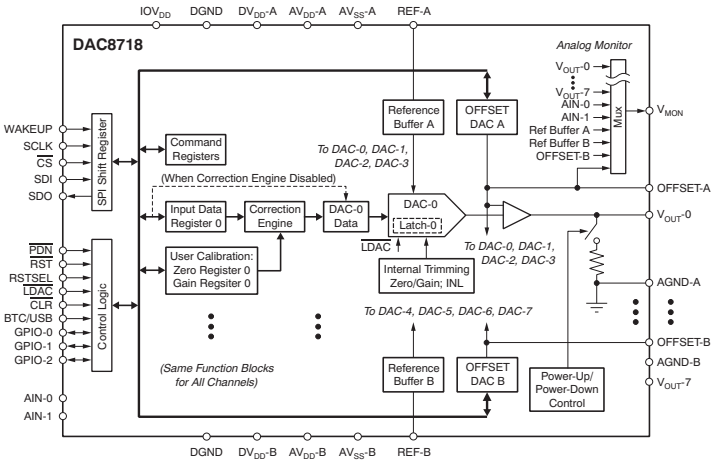
DESCRIPTION

The DAC8718 is a low-power, octal, 16-bit digital-to-analog converter (DAC). The output can be a bipolar ±15-V voltage when operating from a dual ±16.5V power supply, or a unipolar 0-V to +18-V voltage when operating from a +20-V power supply. This DAC provides low-power operation, good linearity, and low glitch over the specified temperature range of –40°C to +105°C. This device is trimmed in manufacturing and has very low zero-code and gain error. In addition, system level calibration can be performed to achieve ±1 LSB zero-code and gain error over entire signal chain. The output range can be offset by properly setting the DAC offset register.

The DAC8718 features a standard, high-speed serial peripheral interface (SPI) at up to 50 MHz and 1.8-V, 3-V, and 5-V logic compatible, to communicate with a DSP or microprocessor. The input data of the device are double-buffered. An asynchronous load input ($\overline{LDAC}$) transfers data from the DAC data register to the DAC latch. The asynchronous CLR input sets the output of all eight DACs to AGND. The V_{MON} pin is a monitor output that connects to the individual analog outputs and two external inputs through a multiplexer (mux).

The DAC8718 is pin-to-pin compatible with the DAC8218 (14-bit) and the DAC7718 (12-bit).

PRODUCT PREVIEW



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	MINIMUM RELATIVE ACCURACY (LSB)	DIFFERENTIAL LINEARITY (LSB)	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING
DAC8718	±1	±1	QFN-48	RGZ	–40°C to +105°C	DAC8718
	±1	±1	TGFP-64	PAG	–40°C to +105°C	DAC8718

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this data sheet, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		DAC8718	UNIT
AV_{DD} to AGND		TBD	V
DV_{DD} to DGND		TBD	V
IOV_{DD} to DGND		TBD	V
Digital input voltage to DGND		TBD	V
V_{OUT} to AGND		TBD	V
Operating temperature range		TBD	°C
Storage temperature range		TBD	°C
Maximum junction temperature (T_J max)		TBD	°C
ESD ratings	Human body model (HBM)	TBD	V
	Charged device model (CDM)	TBD	V

(1) Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS: Dual-Supply

All specifications at $T_A = T_{MIN}$ to T_{MAX}, AV_{DD} = +16.5 V, AV_{SS} = –16.5 V, DV_{DD} = +5 V, reference on REF-A and REF-B = +5 V, gain = 6, and AGND-x = DGND = 0V; Offset DAC A and Offset DAC B are at default values, unless otherwise noted.(1)

PARAMETER	CONDITIONS	DAC8718			UNIT
		MIN	TYP	MAX	
STATIC PERFORMANCE					
Bipolar Output					
Resolution		16			Bits
Linearity error				±4	LSB
Differential linearity error				±1	LSB
Bipolar zero error	T_A = +25°C, before user calibration			±10	LSB
Bipolar zero error TC				±5	ppm FSR/°C
Zero-code error	T_A = +25°C, before user calibration			±10	LSB
	T_A = +25°C, after user calibration			±1	LSB
Zero-code error TC				±5	ppm FSR/°C
Gain error	T_A = +25°C, before user calibration			±0.015	% FS
	T_A = +25°C, after user calibration			±0.0015	% FS
Gain error TC				±5	ppm FSR/°C
Full-scale error	T_A = +25°C, before user calibration			±10	LSB
	T_A = +25°C, after user calibration			±1	LSB
Full-scale error TC				±5	ppm FSR/°C
DC crosstalk(2)				0.1	LSB

(1) Offset DAC A and Offset DAC B are trimmed in manufacturing to minimize the error for symmetrical output. The default value may vary no more than ±10 LSB from the nominal number listed in Table 3.

(2) The DAC outputs are buffered by op amps that share common AV_{DD} and AV_{SS} power supplies. DC crosstalk indicates how much dc change in one or more channel outputs may occur when the dc load current changes in one channel (because of an update). With high-impedance loads, the effect is virtually immeasurable. Multiple V_{DD} and V_{SS} terminals are provided to minimize dc crosstalk.

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS: Dual-Supply (continued)

All specifications at $T_A = T_{MIN}$ to T_{MAX}, AV_{DD} = +16.5 V, AV_{SS} = –16.5 V, DV_{DD} = +5 V, reference on REF-A and REF-B = +5 V, gain = 6, and AGND-x = DGND = 0V; Offset DAC A and Offset DAC B are at default values, unless otherwise noted.

PARAMETER	CONDITIONS	DAC8718			UNIT
		MIN	TYP	MAX	
ANALOG OUTPUT (V_{OUT}-0 to V_{OUT}-7)					
Voltage output(3)	V_{REF} = +5 V, Offset DAC output = 3 V	–15		+15	V
	V_{REF} = +1.5 V, Offset DAC output = 0.9V	–4.5		+4.5	V
Output impedance				0.5	Ω
Short-circuit current(4)			10		mA
Load current				±1	mA
Capacitor load				500	pF
Settling time	To 0.03% of FS, C_L = 200 pF, R_L= 10 kΩ, code from 0000h to FFFFh and FFFFh to 0000h in USB format		10		µs
	To 1 LSB, C_L = 200 pF, R_L = 10 kΩ, code from 0000h to FFFFh and FFFFh to 0000h in USB format		20		µs
Slew rate(5)			5		V/µs
Digital-to-analog glitch(6)	Code from 7FFFh to 8000h and 8000h to 7FFFh		1	TBD	nV-s
Glitch impulse peak amplitude				10 (TBD)	mV
Glitch impulse in power-on(7)	AV_{DD} and AV_{SS} ramp up, 0 to final			TBD (300 ?)	mV
Channel-to-channel isolation(8)			100		dB
DAC-to-DAC crosstalk(9)	DACs in the same group		40		nV-s
	DACs among different groups		10		nV-s
Digital crosstalk(10)			0.1		nV-s
Digital feedthrough(11)			0.6		nV-s
Output noise	T_A = +25°C at 10 kHz, gain = 6		220		nV/√Hz
	T_A = +25°C at 10 kHz, gain = 4		160		nV/√Hz
	0.1 Hz to 10 Hz, gain = 6		20		μV_{PP}
	0.1 Hz to 100 kHz		TBD		μV_{RMS}
Power-supply rejection(12)	V_{DD} = ±5 V to ±16.5 V		0.1	TBD	LSB
OFFSET DAC OUTPUT(13)					
Zero-code error				±10	LSB
Voltage output drift				5	ppm FSR/°C
ANALOG MONITOR PIN (V_{MON})					
Output impedance	T_A = +25°C		1000(14)		Ω
Three-state leakage current			100		nA
Continuous current limit				5	mA

(3) The analog output range of V_{OUT}-0 to V_{OUT}-7 is equal to (6 × V_{REF} – 5 × OUTPUT_OFFSET_DAC) for gain = 6. The maximum value of the analog output must not be greater than (AV_{DD} – 0.5 V), and the minimum value must not be less than (AV_{SS} + 0.5 V). All specifications are for a ±16.5-V power supply and a ±15-V output, unless otherwise noted.
(4) When the output current is greater than the specification, the current is clamped at the specified maximum value.
(5) Slew rate is measured from 10% to 90% of the transition when the output changes from 0 to full-scale.
(6) Digital-to-analog glitch is defined as the amount of energy injected into the analog output at the major code transition. It is specified as the area of the glitch in nV-s. It is measured by toggling the DAC register data between 7FFFh and 8000h in straight binary format.
(7) Power-on glitch is defined as the glitch on V_{OUT} when AV_{DD} and AV_{SS} ramp up from 0 to the final value; ramp time 100 µs.
(8) Channel-to-channel isolation refers to the proportion of input signal from one DAC reference input that appears at the output of another DAC operating from another reference. It is expressed in dB and measured at midscale.
(9) DAC-to-DAC crosstalk is the glitch impulse that appears at the output of one converter as a result of both the digital change and subsequent analog output change at another converter.
(10) Digital crosstalk is the glitch impulse transferred to the output of one converter as a result of a change in the DAC code of another converter.
(11) When the device is not selected, high-frequency logic activity on the device digital inputs can be capacitively coupled both across and through the device to show up as noise on the V_{OUT} pins (it can also be coupled along the supply and ground lines). This noise is digital feedthrough.
(12) The output must not be greater than (AV_{DD} – 0.5 V) and not less than (AV_{SS} + 0.5 V).
(13) Offset DAC A and Offset DAC B are trimmed in manufacturing to minimize the error for symmetrical output. The default value may vary no more than ±10 LSB from the nominal number listed in Table 3.
(14) 5000 Ω when V_{MON} is connected to Reference Buffer A or B.

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS: Dual-Supply (continued)

All specifications at $T_A = T_{MIN}$ to T_{MAX}, AV_{DD} = +16.5 V, AV_{SS} = –16.5 V, DV_{DD} = +5 V, reference on REF-A and REF-B = +5 V, gain = 6, and AGND-x = DGND = 0V; Offset DAC A and Offset DAC B are at default values, unless otherwise noted.

PARAMETER	CONDITIONS	DAC8718			UNIT
		MIN	TYP	MAX	
AUXILIARY ANALOG INPUT (AIN-0, AIN-1) (TBD)					
Input range		TBD	TBD	TBD	V
Input impedance		TBD	TBD	TBD	kΩ
Input capacitance			2.5		pF
Input leakage current		TBD	TBD	TBD	nA
REFERENCE INPUT					
Reference input voltage range(15)		1.5		5.5	V
Reference input dc impedance			100		MΩ
Reference input capacitance			10		pF
DIGITAL INPUT					
High-level input voltage, V_{IH}	IOV_{DD} = +5 V	2.4		0.3 + IOV_{DD}	V
	IOV_{DD} = +3.3 V	2.0		0.3 + IOV_{DD}	V
	IOV_{DD} = +1.8 V	0.95 × IOV_{DD}		0.3 + IOV_{DD}	V
Low-level input voltage, V_{IL}	IOV_{DD} = +5 V	DGND		0.8	V
	IOV_{DD} = +3.3 V	DGND		0.6	V
	IOV_{DD} = +1.8 V	DGND		0.35 × IOV_{DD}	V
Input current				±1	µA
Input capacitance				5	pF
Power-on delay	From AV_{DD} ≥ +4 V and DV_{DD} ≥ +1.6 V to $\overline{CS}$ low			200(16)	µs
Power-down recovery time	From $\overline{RST}$ and $\overline{PDN}$ low-to-high transition to $\overline{CS}$ low			50	µs
DIGITAL OUTPUT					
High-level output voltage, V_{OH}	Sourcing 200 µA	IOV_{DD} – 0.5		IOV_{DD}	V
Low-level output voltage, V_{OL}	Sinking 200 µA			0.4	V
High-impedance leakage				5	µA
High-impedance output capacitance			10		pF
POWER SUPPLY					
AV_{DD}		+5		+18	V
AV_{SS}		–18		–5	V
AI_{DD}	Normal operation			8	mA
AI_{SS}	Normal operation			8	mA
DV_{DD}(17)		+2.7		+5.5	V
IOV_{DD}		+1.8		+5.5	V
Power dissipation	Normal operation, AV_{DD} = +12 V, AV_{SS} = –12 V			192	mW
TEMPERATURE RANGE					
Specified performance		–40		+105	°C

(15) All specifications are for (V_{REF} + 3 V) to +5 V.
(16) The power-on delay is 200 µS max for 100 µS of the power supply ramp time (from 0 V to final value).
(17) When V_{REF} is less than +2.5 V, DV_{DD} must be not less than +2.5 V.

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ELECTRICAL CHARACTERISTICS: Single-Supply

All specifications at $T_A = T_{MIN}$ to T_{MAX}, AV_{DD} = +20 V, AV_{SS} = 0 V, DV_{DD} = +5 V, reference on REF-A and REF-B = +3 V, gain = 6, and AGND-x = DGND = 0V, unless otherwise noted.

PARAMETER	CONDITIONS	DAC8718			UNIT
		MIN	TYP	MAX	
STATIC PERFORMANCE					
Resolution		16			Bits
Linearity error				±4	LSB
Differential linearity error				±1	LSB
Zero-code error	T_A = +25°C, before user calibration			±10	LSB
	T_A = +25°C, after user calibration, code not less than 1024			±1	LSB
Zero-code error TC				±5	ppm FSR/°C
Gain error	T_A = +25°C, before user calibration			±0.015	% FS
	T_A = +25°C, after user calibration			±0.0015	% FS
Gain error TC				±5	ppm FSR/°C
Full-scale error	T_A = +25°C, before user calibration			±10	LSB
	T_A = +25°C, after user calibration			±1	LSB
Full-scale error TC				±5	ppm FSR/°C
DC crosstalk(1)				0.1	LSB
ANALOG OUTPUT (V_{OUT}-0 to V_{OUT}-7)					
Voltage output(2)	V_{REF} = +3 V	0		+18	V
	V_{REF} = +1.5 V	0		+9	V
Output impedance				0.5	Ω
Short-circuit current(3)			10		mA
Load current				±1	mA
Capacitor load				500	pF
Settling time	To 0.03% of FS, C_L = 200 pF, R_L= 10 kΩ, code from 0000h to FFFFh and FFFFh to 0000h in USB format		10		µs
	To 1 LSB, C_L = 200 pF, R_L = 10 kΩ, code from 0000h to FFFFh and FFFFh to 0000h in USB format		20		µs
Slew rate(4)			5		V/µs
Digital-to-analog glitch(5)	Code from 7FFFh to 8000h and 8000h to 7FFFh		1	TBD	nV-s
Glitch impulse peak amplitude	Code from 7FFFh to 8000h and 8000h to 7FFFh			10	mV
Glitch impulse in power-on(6)	AV_{DD} ramps up, 0 to final			TBD (300 ?)	mV
Channel-to-channel isolation(7)			100		dB
DAC-to-DAC crosstalk(8)	DACs in the same group		40		nV-s
	DACs among different groups		10		nV-s
Digital crosstalk(9)			0.1		nV-s
Digital feedthrough(10)			0.6		nV-s

(1) The DAC outputs are buffered by op amps that share common AV_{DD} and AV_{SS} power supplies. DC crosstalk indicates how much dc change in one or more channel outputs may occur when the dc load current changes in one channel (because of an update). With high-impedance loads, the effect is virtually immeasurable. Multiple V_{DD} and V_{SS} terminals are provided to minimize dc crosstalk.
(2) The analog output range of V_{OUT}-0 to V_{OUT}-7 is equal to ($6 \times V_{REF}$) for gain = 6. The maximum value of the analog output must not be greater than (AV_{DD} – 0.5 V). All specifications are for a +20-V power supply and a 0-V to +18-V output, unless otherwise noted.
(3) When the output current is greater than the specification, the current is clamped at the specified maximum value.
(4) Slew rate is measured from 10% to 90% of the transition when the output changes from 0 to full-scale.
(5) Digital-to-analog glitch is defined as the amount of energy injected into the analog output at the major code transition. It is specified as the area of the glitch in nV-s. It is measured by toggling the DAC register data between 7FFFh and 8000h in straight binary format.
(6) Power-on glitch is defined as the glitch on V_{OUT} when AV_{DD} ramps up from 0 to the final value; ramp time is 100 µs.
(7) Channel-to-channel isolation refers to the proportion of input signal from one DAC reference input that appears at the output of another DAC operating from another reference. It is expressed in dB and measured at midscale.
(8) DAC-to-DAC crosstalk is the glitch impulse that appears at the output of one converter as a result of both the digital change and subsequent analog output change at another converter.
(9) Digital crosstalk is the glitch impulse transferred to the output of one converter as a result of a change in the DAC code of another converter.
(10) When the device is not selected, high-frequency logic activity on the device digital inputs can be capacitively coupled both across and through the device to show up as noise on the V_{OUT} pins (it can also be coupled along the supply and ground lines). This noise is digital feedthrough.

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS: Single-Supply (continued)

All specifications at $T_A = T_{MIN}$ to T_{MAX}, AV_{DD} = +20 V, AV_{SS} = 0 V, DV_{DD} = +5 V, reference on REF-A and REF-B = +3 V, gain = 6, and AGND-x = DGND = 0V, unless otherwise noted.

PARAMETER	CONDITIONS	DAC8718			UNIT
		MIN	TYP	MAX	
Output noise	T_A = +25°C at 10 kHz, gain = 6		220		nV/√Hz
	T_A = +25°C at 10 kHz, gain = 4		160		nV/√Hz
	0.1 Hz to 10 Hz, gain = 6		20		μV_{PP}
	0.1 Hz to 100 kHz		TBD		μV_{RMS}
Power-supply rejection(11)	V_{DD} = TBD		0.1	TBD	LSB
ANALOG MONITOR PIN (V_{MON})					
Output impedance	T_A = +25°C		1000(12)		Ω
Three-state leakage current			100		nA
Continuous current limit				5	mA
AUXILIARY ANALOG INPUT (AIN-0, AIN-1) (TBD)					
Input range		TBD	TBD	TBD	V
Input impedance		TBD	TBD	TBD	kΩ
Input capacitance			2.5		pF
Input leakage current		TBD	TBD	TBD	nA
REFERENCE INPUT					
Reference input voltage range(13)		1.5		5.5	V
Reference input dc impedance			100		MΩ
Reference input capacitance			10		pF
DIGITAL INPUT					
High-level input voltage, V_{IH}	IOV_{DD} = +5 V	2.4		0.3 + IOV_{DD}	V
	IOV_{DD} = +3.3 V	2.0		0.3 + IOV_{DD}	V
	IOV_{DD} = +1.8 V	0.95 × IOV_{DD}		0.3 + IOV_{DD}	V
Low-level input voltage, V_{IL}	IOV_{DD} = +5 V	DGND		0.8	V
	IOV_{DD} = +3.3 V	DGND		0.6	V
	IOV_{DD} = +1.8 V	DGND		0.35 × IOV_{DD}	V
Input current				±1	µA
Input capacitance				5	pF
Power-on delay	From AV_{DD} ≥ +4 V and DV_{DD} ≥ +1.6 V to $\overline{CS}$ low			200(14)	µs
Power-down recovery time	From $\overline{RST}$ and $\overline{PDN}$ low-to-high transition to $\overline{CS}$ low			50	µs
DIGITAL OUTPUT					
High-level output voltage, V_{OH}	Sourcing 200 µA	IOV_{DD} – 0.5		IOV_{DD}	V
Low-level output voltage, V_{OL}	Sinking 200 µA			0.4	V
High-impedance leakage				5	µA
High-impedance output capacitance			10		pF
POWER SUPPLY					
AV_{DD}		+5		+20	V
AI_{DD}	Normal operation			8	mA
DV_{DD}(15)		V_{REF}		+5.5	V
IOV_{DD}		+1.8		+5.5	V
Power dissipation	Normal operation, AV_{DD} = +20 V			160	mW
TEMPERATURE RANGE					
Specified performance		–40		+105	°C

(11) The analog output must not be greater than (AV_{DD} – 0.5 V).
(12) 5000 Ω when V_{MON} is connected to Reference Buffer A or B.
(13) All specifications are for (V_{REF} + 3 V) to +5 V.
(14) The power-on delay is 200 µS max for 100 µS of the power supply ramp time (from 0 V to final value).
(15) When V_{REF} is less than +2.5 V, DV_{DD} must be not less than +2.5 V.

PRODUCT PREVIEW

FUNCTIONAL BLOCK DIAGRAM

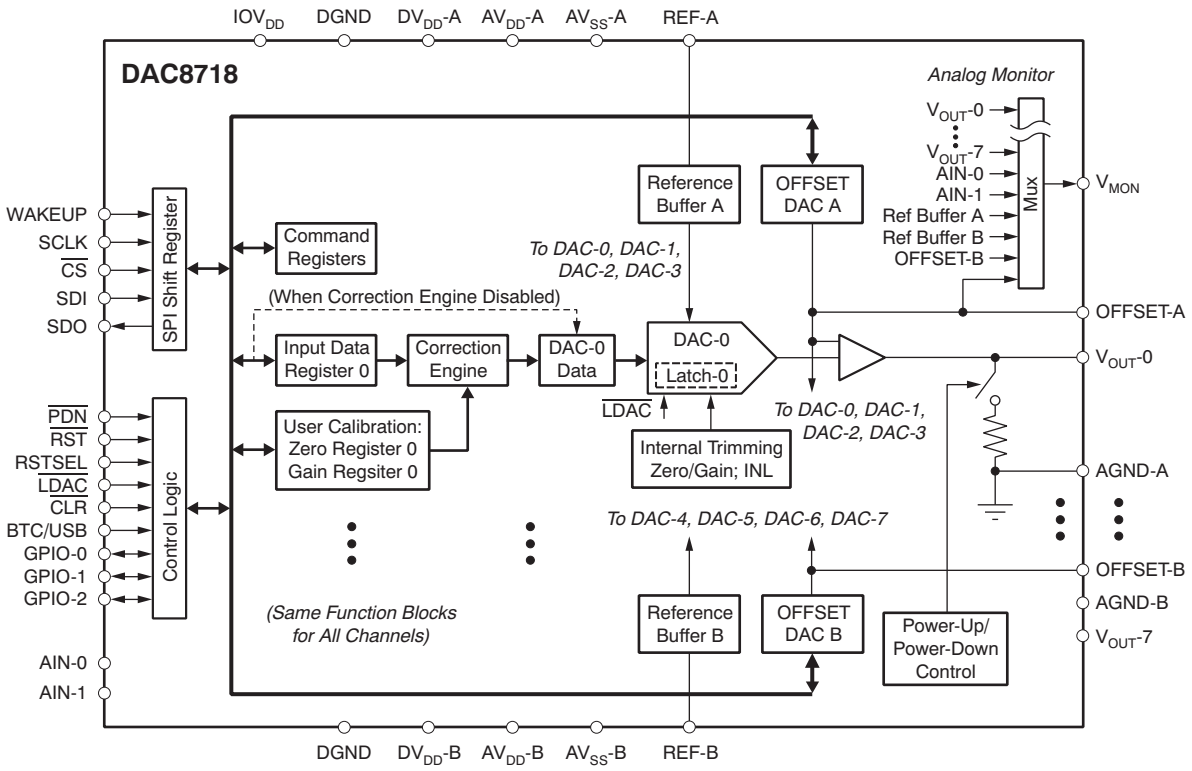
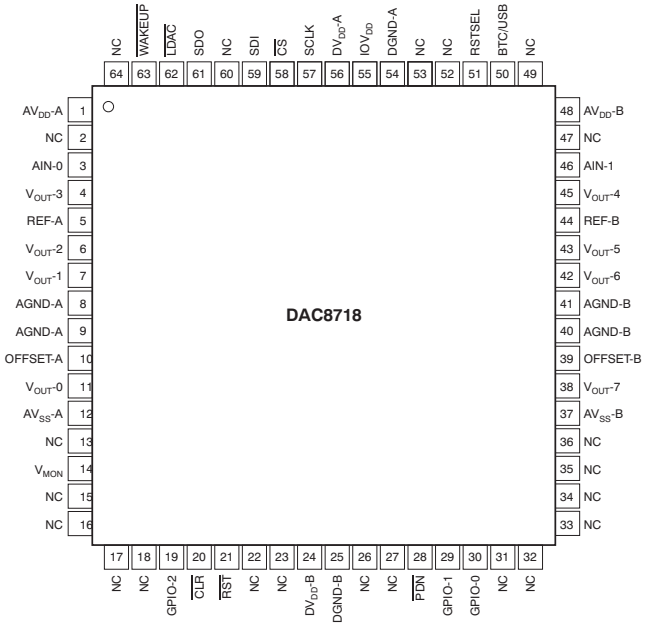


Figure 1. Functional Block Diagram

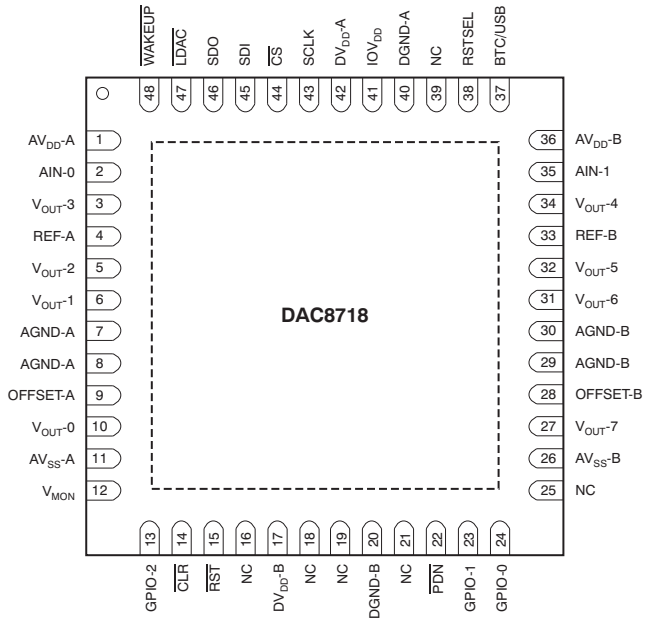
PRODUCT PREVIEW

PIN CONFIGURATIONS

PAG PACKAGE
TQFP-64
(TOP VIEW)



RGZ PACKAGE[1]
QFN-48
(TOP VIEW)



(1) The thermal pad is internally connected to the substrate. This pad can be connected to the analog ground or left floating. Keep the thermal pad separate from the digital ground, if possible.

PIN DESCRIPTIONS

PIN NAME	PIN NO.		I/O	DESCRIPTION
	QFN-48	TQFP-64		
AV_{DD}-A	1	1	I	Group A[1] positive +15-V analog power supply
AIN-0	2	3	I	Auxiliary analog input 0, directly routed to the analog mux
V_{OUT}-3	3	4	O	DAC-3 output
REF-A	4	5	I	Group A reference input
V_{OUT}-2	5	6	O	DAC-2 output
V_{OUT}-1	6	7	O	DAC-1 output
AGND-A	7	8	I	Group A analog ground
AGND-A	8	9	I	Group A analog ground
OFFSET-A	9	10	O	OFFSET DAC-A analog output. Must be connected to AGND-A during single power-supply operation (AV_{SS} = 0 V).
V_{OUT}-0	10	11	O	DAC-0 output
AV_{SS}-A	11	12	I	Group A negative –15-V analog power supply
V_{MON}	12	14	O	Analog monitor output. This pin is either in Hi-Z status, connected to one of the eight DAC outputs, or one of the auxiliary analog inputs, depending on the content of the Monitor Register. See the Monitor Register, Table 8, for details.
GPIO-2	13	19	I/O	General-purpose digital input/output 2. This pin is a bidirectional digital input/output, open-drain. See the *GPIO Pins* section for details.
$\overline{CLR}$	14	20	I	Level Trigger. When the $\overline{CLR}$ pin is logic '0', all V_{OUT}-X pins connect to AGND-x through switches and internal low-impedance. When the $\overline{CLR}$ pin is logic '1', all V_{OUT}-X pins connect to the amplifier outputs.
$\overline{RST}$	15	21	I	Reset input (active low). Logic low on this pin resets the input registers and DACs to the values defined by the RSTSEL pin.

(1) Group A consists of DAC-0, DAC-1, DAC-2, and DAC-3. Group B consists of DAC-4, DAC-5, DAC-6, and DAC-7.

PRODUCT PREVIEW

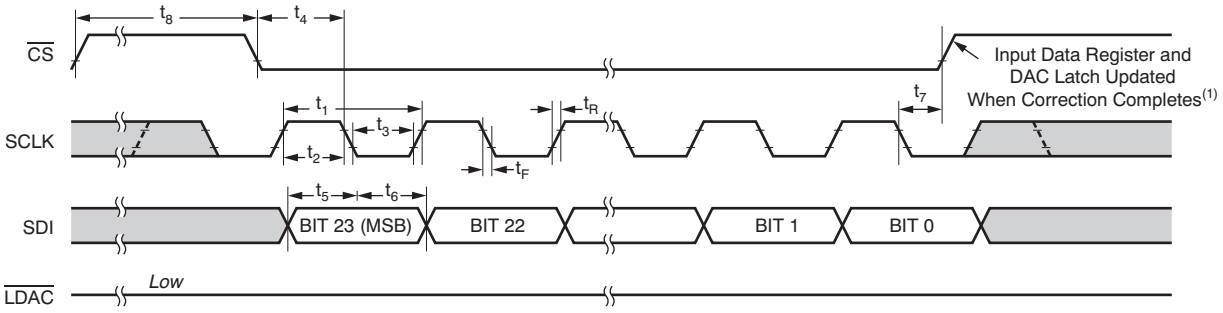
PIN DESCRIPTIONS (continued)

PIN NAME	PIN NO.		I/O	DESCRIPTION
	QFN-48	TQFP-64		
DV_{DD}-B	17	24	I	Goup B[(1)] digital power
DGND-B	20	25	I	Group B digital ground
$\overline{PDN}$	22	28	I	Power-down control input (active low). Logic low on this pin forces the device into a power-down state. During power-down, V_{OUT} connects to AGND through a low impedance.
GPIO-1	23	29	I/O	General-purpose digital input/output 1. This pin is a bidirectional digital input/output, open-drain. See the *GPIO Pins* section for details.
GPIO-0	24	30	I/O	General-purpose digital input/output 0. This pin is a bidirectional digital input/output, open-drain. See the *GPIO Pins* section for details.
AV_{SS}-B	26	37	I	Group B negative –15-V analog power supply
V_{OUT}-7	27	38	O	DAC-7 output
OFFSET-B	28	39	O	OFFSET DAC-B analog output. Must be connected to AGND-B during single-supply operation (AV_{SS} = 0 V).
AGND-B	29	40	I	Group B analog ground
AGND-B	30	41	I	Group B analog ground
V_{OUT}-6	31	42	O	DAC-6 output
V_{OUT}-5	32	43	O	DAC-5 output
REF-B	33	44	I	Group B reference input
V_{OUT}-4	34	45	O	DAC-4 output
AIN-1	35	46	I	Auxiliary analog input 1, directly routed to the analog mux
AV_{DD}-B	36	48	I	Group B positive +15-V analog power supply
BTC/USB	37	50	I	Data format selection of Input DAC data and Offset DAC data. Data are in straight binary format when connected to DGND or in twos complement format when connected to IOV_{DD}. The command data are always in straight binary format. Refer to *Input Data Format* section for details.
RSTSEL	38	51	I	Output reset selection. Selects the output voltage on the V_{OUT} pin after power-on or hardware reset. Refer to the *Power-On Reset* section for details.
DGND-A	40	54	I	Group A digital ground
IOV_{DD}	41	55	I	Interface power
DV_{DD}-A	42	56	I	Goup B digital power
SCLK	43	57		SPI bus serial clock input
$\overline{CS}$	44	58		SPI bus chip select input (active low). Data are not clocked into SDI unless $\overline{CS}$ is low. When $\overline{CS}$ is high, SDO is in a high-impedance state and the SCLK and SDI signals are blocked form the device.
SDI	45	59		SPI bus serial data input
SDO	46	61		SPI bus serial data output. When the DSDO bit = '0', the SDO pin works as an output in normal operation. When the DSDO bit = '1', SDO is always in a Hi-Z state, regardless of the $\overline{CS}$ pin status. Refer to the *Timing Diagrams* section for details.
$\overline{LDAC}$	47	62		Load DAC latch control input (active low). When $\overline{LDAC}$ is low, the DAC latch is transparent and the contents of the DAC Data Register are transferred to it. The DAC output changes to the corresponding level simultaneously when the DAC latch is updated. See the *DAC Output Update* section for details.
$\overline{WAKEUP}$	48	63		Wake-up input (active low). Restores the SPI from sleep to normal operation. See the *Daisy-Chain Operation* section for details.
NC	16, 18, 19, 21, 25, 39	2, 13, 15-18, 22, 23, 26, 27, 31-36, 47, 49, 52, 53, 60, 64		Not connected

PRODUCT PREVIEW

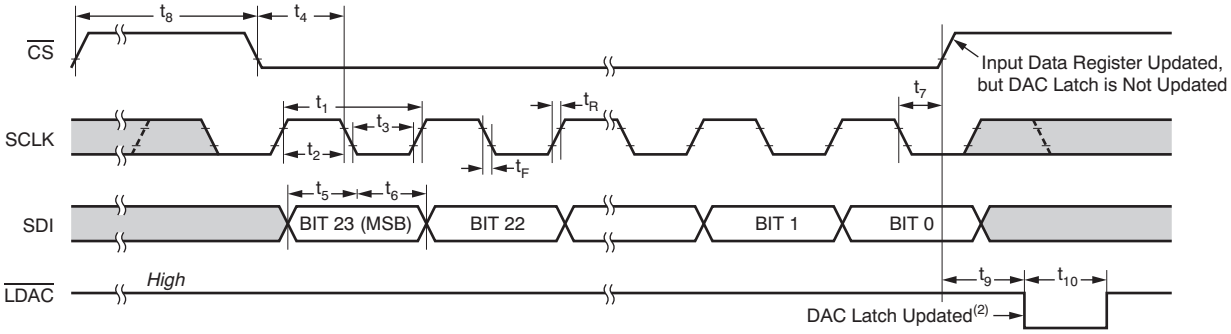
TIMING DIAGRAMS

Case 1: Standalone mode, $\overline{\text{LDAC}}$ tied low.



NOTE: (1) If the correction engine is off, the DAC latch is reloaded immediately after the Input Data Register is updated.

Case 2: Standalone mode, $\overline{\text{LDAC}}$ active high.



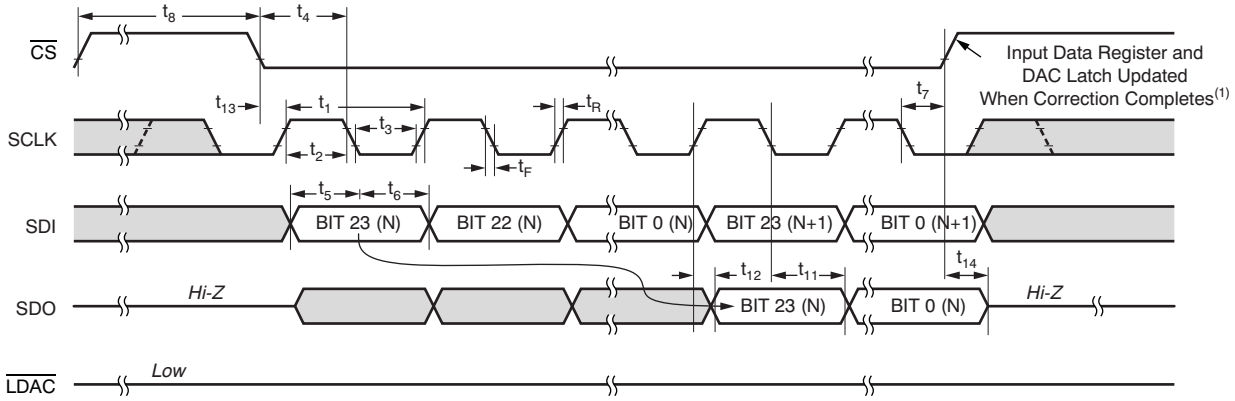
NOTE: (2) The DAC latch is updated when $\overline{\text{LDAC}}$ goes low, as long as the timing requirement of t_9 is satisfied.

Figure 2. SPI Timing for Standalone Mode

PRODUCT PREVIEW

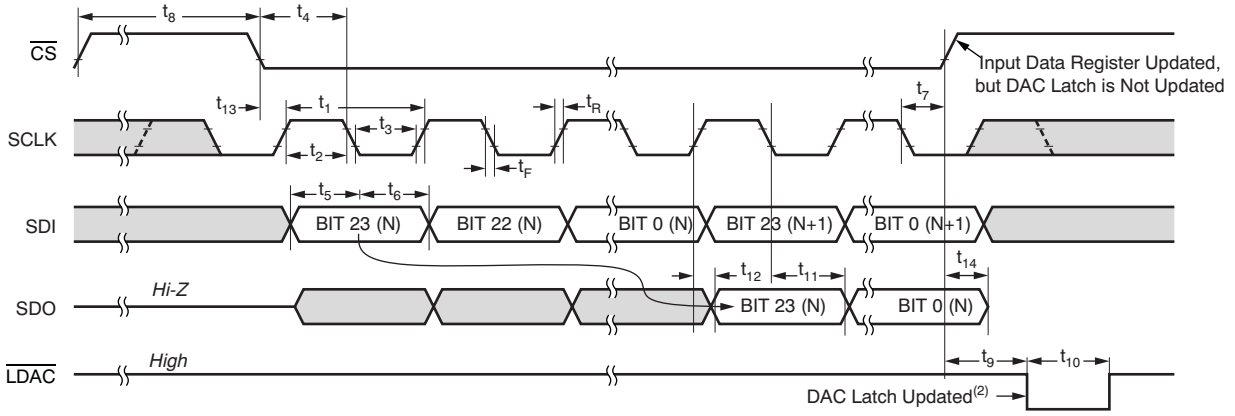
TIMING DIAGRAMS (continued)

Case 3: Daisy-Chain mode, $\overline{\text{LDAC}}$ tied low.



NOTE: (1) If the correction engine is off, the DAC latch is reloaded immediately after the Input Data Register is updated.

Case 4: Daisy-Chain mode, $\overline{\text{LDAC}}$ active.



NOTE: (2) The DAC latch is updated when $\overline{\text{LDAC}}$ goes low. The proper data are loaded if the t9 timing requirement is satisfied. Otherwise, invalid data are loaded.

Case 5: Daisy-Chain mode, sleeping.

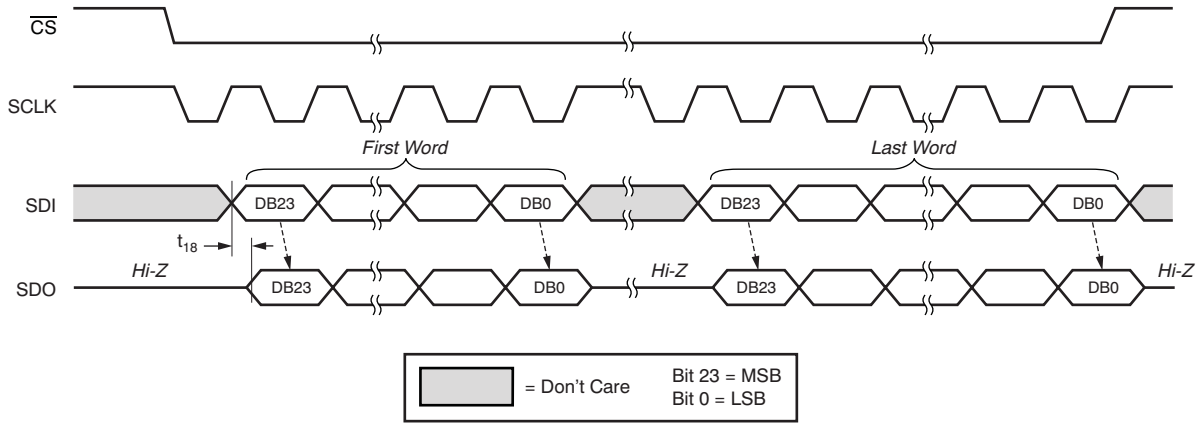


Figure 3. SPI Timing for Daisy-Chain Mode

PRODUCT PREVIEW

TIMING DIAGRAMS (continued)

Case 6: Readback for Standalone mode.

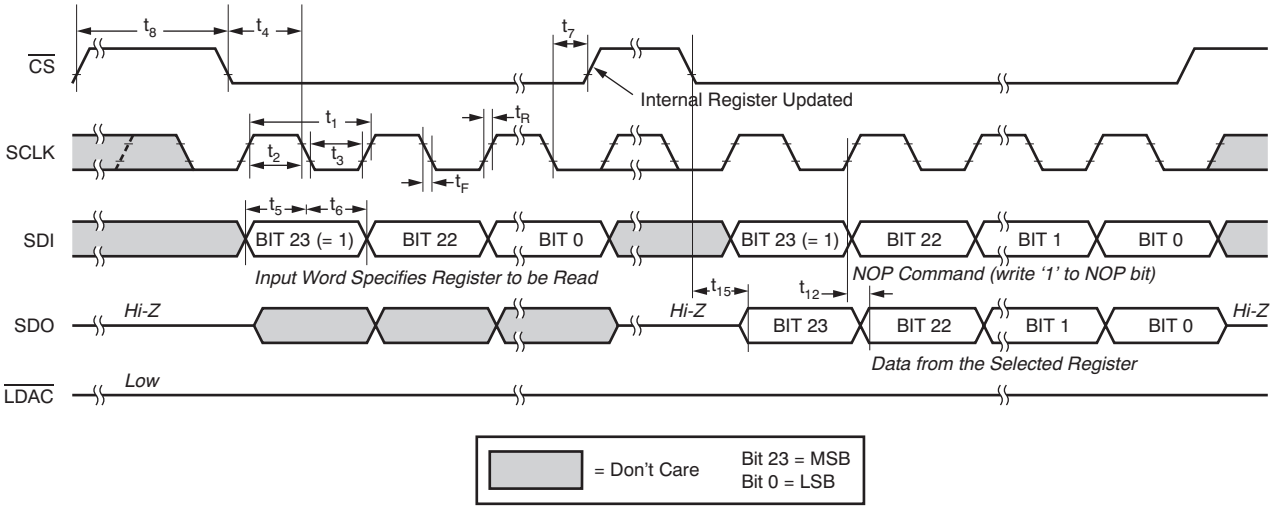


Figure 4. SPI Timing for Readback Operation in Standalone Mode

TIMING CHARACTERISTICS: STANDALONE MODE(1)(2)

At –40°C to +105°C, DV_{DD} = +5 V, and IOV_{DD} = +5 V, unless otherwise noted.

PARAMETER		MIN	MAX	UNIT
f_{SCLK}	Clock frequency		50	MHz
t_1	SCLK cycle time	20		ns
t_2	SCLK high time	7		ns
t_3	SCLK low time	7		ns
t_4	$\overline{CS}$ falling edge to SCLK falling edge setup time	8		ns
t_5	Delay from rising edge of SCLK to SDI valid	2		ns
t_6	SDI hold time after falling edge of SCLK	2		ns
t_7	SCLK falling edge to $\overline{CS}$ rising edge	5		ns
t_8	$\overline{CS}$ high time	10		ns
t_9	$\overline{CS}$ rising edge to $\overline{LDAC}$ falling edge	5		ns
t_{10}	$\overline{LDAC}$ pulse duration	7		ns
t_{12}	Delay from SCLK rising edge to SDO valid	3	8	ns
t_{14}	Delay from $\overline{CS}$ rising edge to SDO Hi-Z	5		ns
t_{15}	Delay from $\overline{CS}$ faliing edge to SDO valid	6		ns
t_{19}	SDO rising/falling time		2	ns

(1) Specified by design. Not production tested.
(2) Sample tested during the initial release and after any redesign or process changes that may affect these parameters.

PRODUCT PREVIEW

TIMING CHARACTERISTICS: DAISY-CHAIN MODE(1)(2)

At –40°C to +105°C, DV_{DD} = +5 V, and IOV_{DD} = +5 V, unless otherwise noted.

PARAMETER		MIN	MAX	UNIT
f_{SCLK}	Clock frequency		50	MHz
t_1	SCLK cycle time	20		ns
t_2	SCLK high time	7		ns
t_3	SCLK low time	7		ns
t_4	$\overline{CS}$ falling edge to SCLK falling edge setup time	8		ns
t_5	Delay from rising edge of SCLK to SDI valid	2		ns
t_6	SDI hold time after falling edge of SCLK	2		ns
t_7	SCLK falling edge to $\overline{CS}$ rising edge	5		ns
t_8	$\overline{CS}$ high time	10		ns
t_9	$\overline{CS}$ rising edge to $\overline{LDAC}$ falling edge	5		ns
t_{10}	$\overline{LDAC}$ pulse duration	7		ns
t_{12}	Delay from SCLK rising edge to SDO valid	3	8	ns
t_{13}	Delay from $\overline{CS}$ falling edge to SCLK rising edge	TBD		ns
t_{14}	Delay from $\overline{CS}$ rising edge to SDO Hi-Z	5		ns
t_{18}	Delay from SDI to SDO in sleep mode	5		ns
t_{19}	SDO rising/falling time		2	ns

(1) Specified by design. Not production tested.
(2) Sample tested during the initial release and after any redesign or process changes that may affect these parameters.

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS: TBD

At T_A = TBD, unless otherwise noted.

PRODUCT PREVIEW

THEORY OF OPERATION

GENERAL DESCRIPTION

The DAC8718 contains eight DAC channels and eight output amplifiers in a single package. Each single channel consists of a resistor-string DAC followed by an output buffer amplifier. The resistor-string section is simply a string of resistors, each with a value of R, from REF to AGND. This type of architecture provides DAC monotonicity. The 16-bit binary digital code loaded to the DAC register determines at which node on the string the voltage is tapped off before being fed into the output amplifier. The output amplifier multiplies the DAC output voltage by a gain of six or four. The output span is 9 V with a 1.5-V reference and 18 V with a 3-V reference and a gain of 6.

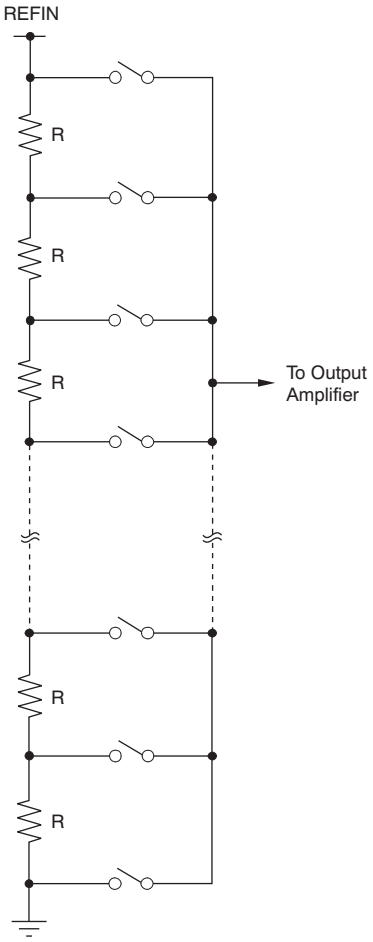


Figure 5. Resistor String

CHANNEL GROUPS

The eight DAC channels are arranged into two groups (A and B) with four channels per group. Group A consists of DAC-0, DAC-1, DAC-2, and DAC-3. Group B consists of DAC-4, DAC-5, DAC-6, and DAC-7. The four DAC channels of Group A derive their reference voltage from REF-A, and those of Group B from REF-B.

USER-CALIBRATION FOR ZERO-CODE ERROR AND GAIN ERROR

The DAC8718 implements a user-calibration function that allows for trimming on the entire signal chain. Each DAC channel has a GAIN Register (or G register) and Zero Register (or Z register). Using the correction engine, the data from the Input Data Register is operated on by a digital multiplier and adder controlled by the contents of Gain and Zero registers. The calibrated DAC data are then stored in the DAC Data Register where they are finally transferred into the DAC latch and set the DAC output. Each time the data are written to the Input Data Register, or to the Gain or Zero register, the data in the Input Data Register is corrected, and the result is automatically transferred to DAC Data Register.

The range of the gain adjustment is 0.5 to 1.5. The range of the zero adjustment is –32768 LSB to +32767 LSB, or ±50% of full scale. There is only one correction engine in the device, which is shared between all channels. It takes about 500 ns per channel for the correction engine to process the data.

If the user-calibration function is not needed, the correction engine can be turned off to speed up the device. Setting the SCE bit in the Configuration Register to '0' turns off the correction engine. Setting SCE to '1' enables the correction engine. When SCE = '0', the data are directly transferred to the DAC Data Register after writing the DAC data into the device. In this case, writing to the Gain Register or Zero Register has no effect; reading these registers returns the existing value.

The data format of the Gain Register is straight binary. The data format of the Zero Register is twos complement. See the *Input Data Format* section for details.

ANALOG OUTPUTS (V_{OUT}-0 to V_{OUT}-7, with Reference to the AGND-x)

When the correction engine is off (SCE = '0'):

$$V_{OUT} = V_{REF} \times Gain \times \left(\frac{INPUT\_CODE}{65536} \right) - V_{REF} \times (Gain - 1) \times \left(\frac{OFFSETDAC\_CODE}{65536} \right) \quad (1)$$

When the correction engine is on (SCE = '1'):

$$V_{OUT} = V_{REF} \times Gain \times \left(\frac{DAC\_DATA\_CODE}{65536} \right) - V_{REF} \times (Gain - 1) \times \left(\frac{OFFSETDAC\_CODE}{65536} \right) \quad (2)$$

Where:

$$DAC\_DATA\_CODE = \left(\frac{INPUT\_CODE \times (USER\_GAIN + 2^{15})}{2^{16}} \right) + USER\_ZERO$$

Gain is the DAC gain defined by the GAIN bit in the Configuration Register.
INPUT_CODE is the data written into the Input Data Register.
OFFSETDAC_CODE is the data written into the Offset DAC.
USER_GAIN is the code of the Gain Register
UZER_ZERO is the code of the Zero Register

For single-supply operation, the Offset DAC output is 0 V, and the Offset DAC code is '0'.

For dual-supply operation, the power-on default value of the Gain Register is 32768, and the default value of the Zero Register is '0'. The default value of the Offset DAC is 39321.

Note that the maximum output voltage must not be greater than (AV_{DD} – 0.5 V) and the minimum output voltage must not be less than (AV_{SS} + 0.5 V); otherwise, the output may be saturated.

INPUT DATA FORMAT

The USB/BTC pin defines the input data format and the Offset DAC format. When this pin connects to DGND, the Input DAC data and Offset DAC data are straight binary, as shown in Table 1. When this pin is connected to IOV_{DD}, the Input DAC data and Offset DAC data are twos complement, as shown in Table 2.

Table 1. Output vs Straight Binary Code for Default Offset DAC (999Ah) and Gain = x6

USB CODE	OUTPUT	DESCRIPTION
FFFFh	$+3 \times V_{REF} \times (32767/32768)$	+Full-Scale – 1 LSB
••• •••	••• •••	••• •••
8001h	$+1.5 \times V_{REF} \times (1/32768)$	+1 LSB
8000h	0	Zero
7FFFh	$-1.5 \times V_{REF} \times (1/32768)$	–1 LSB
••• •••	••• •••	••• •••
0000h	$-3 \times V_{REF} \times (32768/32768)$	–Full-Scale

Table 2. Output vs Twos Complement Code for Default Offset DAC (199Ah) and Gain = x6

BTC CODE	OUTPUT	DESCRIPTION
7FFFh	$+3 \times V_{REF} \times (32767/32768)$	+Full-Scale – 1 LSB
••• •••	••• •••	••• •••
0001h	$+1.5 \times V_{REF} \times (1/32768)$	+1 LSB
0000h	0	Zero
FFFFh	$-1.5 \times V_{REF} \times (1/32768)$	–1 LSB
••• •••	••• •••	••• •••
8000h	$-3 \times V_{REF} \times (32768/32768)$	–Full-Scale

The data written to the Gain Register are always in straight binary, data to the Zero Register are in twos complement, and data to all other control registers are as specified in the definitions, regardless of the USB/BTC pin status.

In reading operation, the read-back data are in the same format as written.

OFFSET DACS

There are two 16-bit Offset DACs: one for Group A, and one for Group B. The Offset DACs allow the output range of all DACs connected to them to be offset within a defined range. Thus, subject to the limitations of headroom, it is possible to set the output range of Group A and/or Group B to be unipolar positive, unipolar negative, or bipolar, and either symmetrical or asymmetrical at about zero volts. The DACs in the DAC8718 are factory trimmed with the Offset DACs set at their default values, providing the best offset and gain performance for the default output range and span. When the output range is adjusted by changing the value of the Offset DAC, an extra offset is introduced as a result of the gain error of the Offset DAC. The amount of this extra offset is dependent on the magnitude of the reference and how much the Offset DAC changes from its default value. The worst-case offset occurs when the Offset DAC is at positive or negative full-scale. The allowed maximum offset depends on the reference and the power supply. In any case, the analog output must not go beyond the specified range shown in the *Analog Outputs* section. After power-on or reset, the Offset DAC is set to the value defined by the selected data format and the selected analog output voltage. Refer to the *Power-On Reset* and *Hardware Reset* sections for details.

For single-supply operation (AV_{SS} = 0 V), the Offset DAC is turned off, and the output amplifier is in a Hi-Z state. The OFFSET-x pin must be connected to the AGND-x pin. For dual-supply operation, this pin provides the output of the Offset DAC.

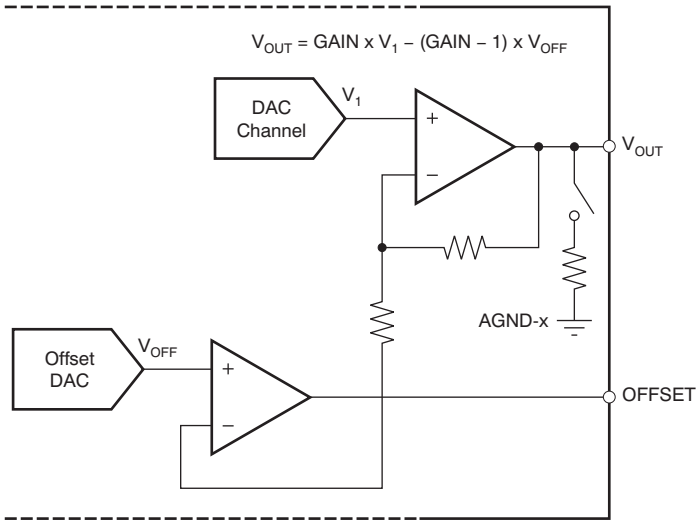


Figure 6. Output Amplifier and Offset DAC

OUTPUT AMPLIFIERS

The output amplifiers can swing to 0.5 V below the positive supply and 0.5 V above the negative supply. This condition limits how much the output can be offset for a given reference voltage. The maximum range of the output for ±17-V power and a +5.5-V reference is –16.5 V to +16.5 V for gain = 6.

Each output amplifier is implemented with individual over-current protection. The amplifier is clamped at 5 mA, even if the output current goes over 5 mA.

PRODUCT PREVIEW

GENERAL-PURPOSE INPUT/OUTPUT PINS (GPIO-0 to GPIO-2)

The GPIO-0, GPIO-1, and GPIO-2 pins are general-purpose, bidirectional, digital input/output (I/O) signals. These pins can receive an input or produce an output. When the GPIO-n pin acts as an output, the status is determined by the corresponding GPIO-n bit of the GPIO Register. The output status is high impedance when the GPIO-n bit is set to '1', and is logic low when the GPIO-n bit is cleared to '0'. Note that an external pullup resistor is required when using the GPIO-n pin as an output.

When the GPIO-n pin acts as input, the digital value on the pin is acquired by reading the GPIO-n bit in the GPIO Register.

After power-on reset or any forced hardware or software reset, all GPIO-n bits are set to '1', thus placing them in a high impedance state.

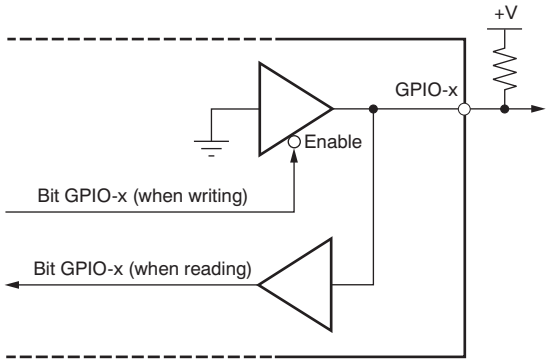


Figure 7. GPIO Pins

ANALOG OUTPUT PIN ($\overline{CLR}$)

The $\overline{CLR}$ pin is an active low input that should be high for normal operation. When this pin is in logic '0', all V_{OUT} outputs connect to AGND-x through internal 20-kΩ resistors and are cleared to 0 V, and the output buffer is in a Hi-Z state. While $\overline{CLR}$ is low, all $\overline{LDAC}$ pulses are ignored. When $\overline{CLR}$ is taken high again while the $\overline{LDAC}$ is high, the DAC outputs remain cleared until $\overline{LDAC}$ is taken low. However, if $\overline{LDAC}$ is tied low, taking $\overline{CLR}$ back to high sets the DAC output to the level defined by the value of the DAC latch. The contents of the Zero Registers, Gain Registers, Input Data Registers, DAC Data Registers, and DAC latches are not affected by taking $\overline{CLR}$ low.

POWER-ON RESET

The DAC8718 contains a power-on reset circuit that controls the output during power-up and power down. This feature is useful in applications where the known state of the DAC output during power-up is important. During power-up all V_{OUT} outputs are connected to ground through an internal 20-kΩ resistors; the Input Data Registers, Offset DAC Registers, DAC Data Registers, and DAC latches are loaded with the value defined by the RSTSEL pin, as shown in Table 3. The Gain Registers and Zero Registers are loaded with default values. When the power is stable, the V_{OUT} outputs change to the new value. However, the SPI Shift Register is not cleared on power-up, so the register contents are undefined.

Table 3. Reset Values for Dual Power-Supply Operation

RSTSEL PIN	BTC/USB PIN	INPUT FORMAT	VALUE OF INPUT DATA REGISTER AND DAC LATCH	VALUE OF OFFSET DAC REGISTER FOR GAIN = 6 (1)	V_{OUT}
DGND	DGND	Straight Binary	0000h	999Ah	–Full-Scale
IOV_{DD}	DGND	Straight Binary	8000h	999Ah	0 V
DGND	IOV_{DD}	Twos Complement	8000h	199Ah	–Full-Scale
IOV_{DD}	IOV_{DD}	Twos Complement	0000h	199Ah	0 V

(1) Offset DAC A and Offset DAC B are trimmed in manufacturing to minimize the error for symmetrical output. The default value may vary no more than ±10 LSB from the nominal number listed in this table.

PRODUCT PREVIEW

In single-supply operation, the Offset DAC is turned off and the output is unipolar. The power-on reset is defined as shown in Table 4.

Table 4. Unipolar Output Reset Values for Single Power-Supply Operation

RSTSEL PIN	BTC/USB PIN	INPUT FORMAT	VALUE OF INPUT DATA REGISTER AND DAC LATCH	V_{OUT}
DGND	DGND	Straight Binary	0000h	0 V
IOV_{DD}	DGND	Straight Binary	8000h	Midscale
DGND	IOV_{DD}	Twos Complement	8000h	0 V
IOV_{DD}	IOV_{DD}	Twos Complement	0000h	Midscale

HARDWARE RESET

When the $\overline{RST}$ pin is low, the device is in hardware reset. All the analog outputs (V_{OUT}-0 to V_{OUT}-7) are connected to the corresponding GNDs through the internal resistor. The Input Data Registers, Offset DACs, and DAC latches are loaded with the value defined by the RSTSEL pin (see Table 3). SPI communication is disabled. The signals on SDI, SCLK and $\overline{CS}$ are ignored, and SDO is in a high-impedance state. On the rising edge of $\overline{RST}$, the analog outputs (V_{OUT}-0 to V_{OUT}-7) are connected to the output amplifier and set to the potential specified by the the RSTSEL pin, if the $\overline{CLR}$ pin is high. After $\overline{RST}$ goes high, the device returns to normal operation.

DAC OUTPUT UPDATE

Depending on the status of both $\overline{CS}$ and $\overline{LDAC}$, and after data have been transferred into the DAC Data registers, the DAC outputs can be updated either in asynchronous mode or synchronous mode. The update mode is established at power-up. If asynchronous mode is desired, the $\overline{LDAC}$ pin must be permanently tied low before power is applied to the device. If synchronous mode is desired, $\overline{LDAC}$ must be logic high before and during power on.

Asynchronous Mode

The $\overline{LDAC}$ pin is permanently tied low, the LD bit is ignored. When the correction engine is off (SCE bit = '0'), DAC Data Registers and DAC latches are updated immediately when $\overline{CS}$ goes high. When the correction engine is on (SCE bit= '1'), each DAC latch is updated when the correction engine updates the corresponding DAC Data Register.

Synchronous Mode

When $\overline{LDAC}$ stays high, the DAC latch is not updated; therefore, the DAC output does not change. The DAC latch is updated by taking $\overline{LDAC}$ low (or setting the LD bit in the Configuration Register to '1') any time after the delay of t_9 from the completion of the write operation. If the timing requirement of t_9 is not satisfied, invalid data are loaded. Refer to the *Timing Diagrams* and the Configuration Register (Table 7) for details.

The DAC8718 updates the DAC latch only if it has been accessed since the last time that $\overline{LDAC}$ was brought low or if the LD bit is set to '1', thereby eliminating unnecessary glitch. Any DAC channels that have not been accessed are not reloaded. When the DAC latch is updated, the corresponding output changes to the new level immediately.

PRODUCT PREVIEW

MONITOR OUTPUT PIN (V_{MON})

The V_{MON} pin is the channel monitor output. It monitors one of the DAC outputs, the reference buffer outputs, the Offset DAC outputs, or two auxiliary external analog inputs on pins AIN-0 and AIN-1. The channel monitor function consists of an analog multiplexer addressed via the serial interface, allowing any one of the monitored signals to be routed to this pin for monitoring using an external analog-to-digital converter (ADC). The monitor function is controlled by the Monitor Register, which allows the monitor output to be enabled or disabled. When disabled, the monitor output is high impedance, so several monitor outputs can be connected in parallel with only one enabled at a time.

Note that the multiplexer is implemented as a series of analog switches. Because this configuration could conceivably cause a large amount of current to flow from the input of the multiplexer (that is, from V_{OUT}-X to the output of the multiplexer, V_{MON}), care should be taken to ensure that it is correctly connected. The V_{MON} pin is of high impedance in order to prevent the continuous current limit specification from being exceeded. Refer to the Monitor Register for more details.

ANALOG INPUT PINS (AIN-0 and AIN-1)

Pins AIN-0 and AIN-1 are two analog inputs that directly connect to the analog mux of the analog monitor output. When AIN-0 or AIN-1 is accessed, it is routed via the mux to the V_{MON} pin. Thus, one external ADC channel can monitor eight DACs plus two extra external analog signals, AIN-0 and AIN-1.

POWER-DOWN MODE

the DAC8718 is implemented with power-down function to reduce power consumption. Either the entire device or each individual group can be put into power-down mode. If the $\overline{PDN}$ pin is connected to DGND, the entire device is put into power-down mode. If the proper power-down bit (PD-x) in the power-down register is set to '1', the individual group is put into power down mode. During power-down mode, the analog outputs (V_{OUT}-0 to V_{OUT}-7) connect to AGND-x through an internal resistor, and the output buffer is in Hi-Z status. When the entire device is in power-down, the bus interface is still active in order to continue communication and receive commands from the host controller, but all other circuits are powered down. The host controller can wake the device from power-down mode and return to normal operation by through either software or hardware; it takes 200 μs or less for recovery to complete.

PRODUCT PREVIEW

SERIAL INTERFACE

The DAC8718 is controlled over a versatile, three-wire serial interface that operates at clock rates of up to 50 MHz and is compatible with SPI, QSPI™, Microwire™, and DSP™ standards.

SPI Shift Register

The SPI Shift Register is 24 bits wide. Data are loaded into the device MSB first as a 24-bit word under the control of the serial clock input, SCLK. The SPI Shift Register consists of a read/write bit, five register address bits, 16 data bits, and two reserve bits for future devices, as shown in Table 5. The falling edge of $\overline{CS}$ starts the communication cycle. The data are latched into the SPI Shift Register on the falling edge of SCLK while $\overline{CS}$ is low. When $\overline{CS}$ is high, the SCLK and SDI signals are blocked and the SDO pin is in a high-impedance state. The contents of the SPI shifter register are decoded and transferred to the proper internal registers on the rising edge of $\overline{CS}$. The timing for this operation is shown in the *Timing Diagrams* section.

The serial interface works with both a continuous and non-continuous serial clock. A continuous SCLK source can only be used if $\overline{CS}$ is held low for the correct number of clock cycles. In gated clock mode, a burst clock containing the exact number of clock cycles must be used and $\overline{CS}$ must be taken high after the final clock in order to latch the data.

Stand-Alone Operation

The serial clock can be a continuous or a gated clock. The first falling edge of $\overline{CS}$ starts the operation cycle. Exactly 24 falling clock edges must be applied before $\overline{CS}$ is brought back high again. If $\overline{CS}$ is brought high before the 24th falling SCLK edge, then the data written are not transferred into the internal registers. If more than 24 falling SCLK edges are applied before $\overline{CS}$ is brought high, then the last 24-bits are used. The device internal registers are updated from the Shift Register on the rising edge of $\overline{CS}$. In order for another serial transfer to take place, $\overline{CS}$ must be brought low again.

When the data have been transferred into the chosen register of the addressed DAC, all DAC registers and analog outputs can be updated by taking $\overline{LDAC}$ low.

Daisy-Chain Operation

For systems that contain more than one device, the SDO pin can be used to daisy-chain multiple devices together. Daisy-chain operation can be useful in system diagnostics and in reducing the number of serial interface lines. Note that before daisy-chain operation can begin, the SDO pin must be enabled by setting the SDO disable bit (DSDO) in the Configuration Register to '0'; this bit is cleared by default.

The DAC8718 provides two modes for daisy-chain operation: normal and sleep. The SLEEP bit in the SPI Mode register determines which mode is used.

In Normal mode (SLEEP bit = '0'), the data clocked into the SDI pin are transferred into the Shift Register. The first falling edge of $\overline{CS}$ starts the operating cycle. SCLK is continuously applied to the SPI Shift Register when $\overline{CS}$ is low. If more than 24 clock pulses are applied, the data ripple out of the Shift Register and appear on the SDO line. These data are clocked out on the rising edge of SCLK and are valid on the falling edge. By connecting the SDO pin of the first device to the SDI input of the next device in the chain, a multiple-device interface is constructed. Each device in the system requires 24 clock pulses. Therefore, the total number of clock cycles must equal 24 × N, where *N* is the total number of DAC8718s in the chain. When the serial transfer to all devices is complete, $\overline{CS}$ is taken high. This action latches the data from the SPI Shift Registers to the device internal registers for each device in the daisy-chain, and prevents any further data from being clocked in. The serial clock can be a continuous or a gated clock. Note that a continuous SCLK source can only be used if $\overline{CS}$ is held low for the correct number of clock cycles. For gated clock mode, a burst clock containing the exact number of clock cycles must be used and $\overline{CS}$ must be taken high after the final clock in order to latch the data.

In Sleep mode (SLEEP bit = '1'), the data clocked into SDI are routed to the SDO pin directly; the Shift Register is bypassed. The first falling edge of $\overline{CS}$ starts the operating cycle. When SCLK is continuously applied with $\overline{CS}$ low, the data clocked into the SDI pin appear on the SDO pin almost immediately (with approximately a 5 ns delay; see the *Timing Diagrams* section); there is no 24 clock delay, similar to normal operting mode. While in Sleep mode, no data bits are clocked into the Shift Register, and the device does not receive any new data or commands. Putting the device into Sleep mode eliminates the 24 clock delay from SDI to SDO caused by the

Shift Register, thus greatly speeding up the data transfer. For example, consider three DAC8718s (A, B, and C) in a daisy-chain configuration. The data from the SPT controller are transferred first to A, then to B, and finally to C. In normal daisy-chain operation, a total of 72 clocks are needed to transfer one word to C. However, if A and B are placed into Sleep mode, the first 24 data bits are directly transferred to C (through A and B); therefore, only 24 clocks are needed.

To wake the device up from sleep mode and return to normal operation, either one of following methods can be used:

1. Pull the $\overline{\text{WAKEUP}}$ pin low, which forces the SLEEP bit to '0' and returns the device to normal operating mode.
2. Use the W2 bit and the $\overline{\text{CS}}$ pin.

When the W2 bit = '1', if $\overline{\text{CS}}$ is applied with no more than one falling edge of SCLK, then the rising edge of $\overline{\text{CS}}$ wakes the device from sleep mode back to normal operation. However, the device will not wake-up if more than one falling edge of SCLK exists while $\overline{\text{CS}}$ is low.

Read-Back Operation

The READ command is used to start read-back operation. However, before read-back operation can be initiated, the SDO pin must be enabled by setting the DSDO bit in the Configuration Register to '0'; this bit is cleared by default. Read-back operation is then started by executing a READ command (R/W bit = '1', see Table 5). Bits A4 to A0 in the READ command select the register to be read. The remaining data in the command are don't care bits. During the next SPI operation, the data appearing on the SDO output are from the previously addressed register. For a read of a single register, a NOP command can be used to clock out the data from the selected register on SDO. Multiple registers can be read if multiple READ commands are issued. The readback diagram in Figure 8 shows the read-back sequence.

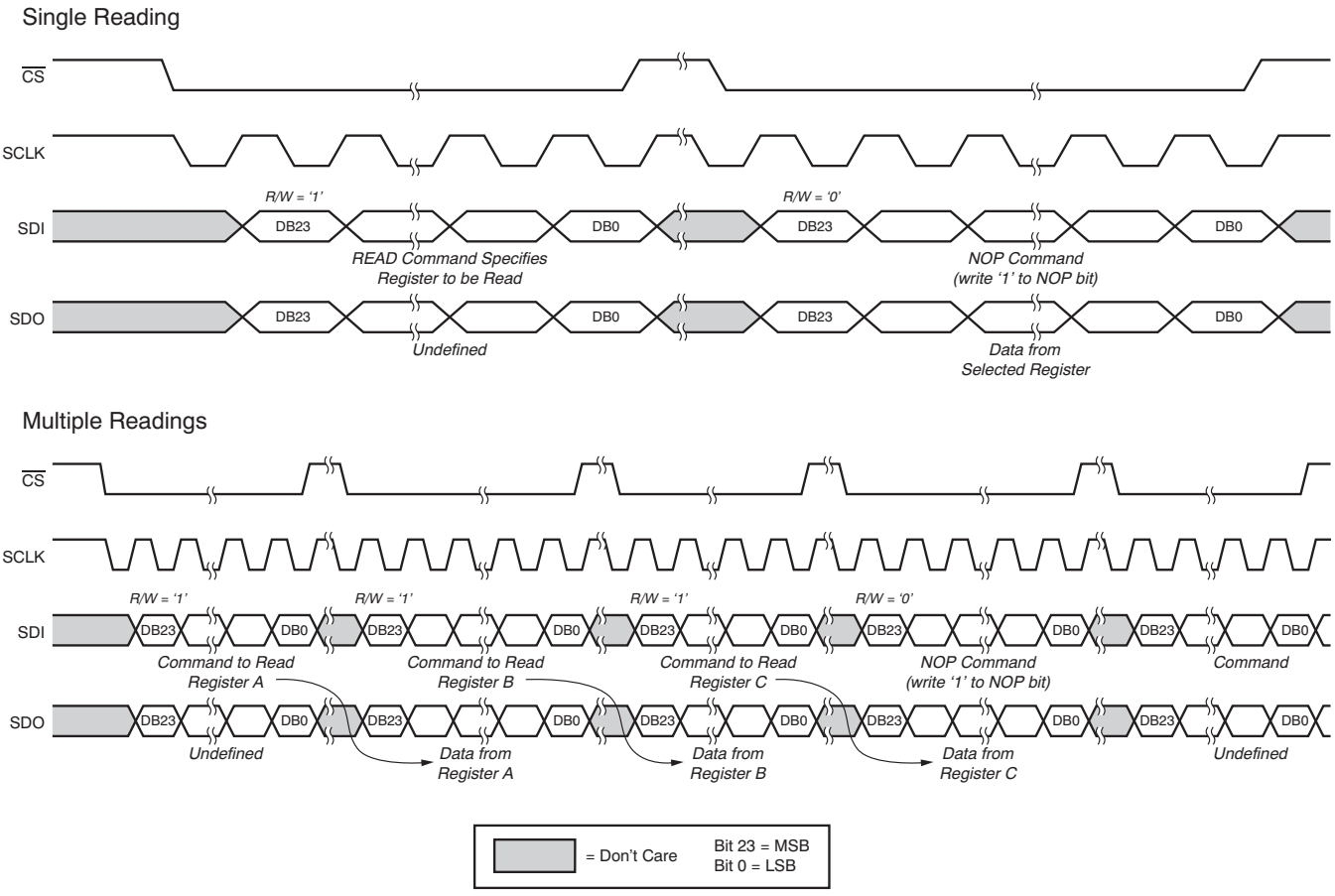


Figure 8. Read-Back Operation

PRODUCT PREVIEW

SPI SHIFT REGISTER

The SPI Shift Register is 24 bits wide, as shown in Table 5. The register mapping is shown in Table 6; x = don't care—writing to it has no effect, reading it returns '0'.

Table 5. Shift Register Format

MSB								
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15:DB0
R/W	X	X	A4	A3	A2	A1	A0	DATA

R/W—Indicates a read from or a write to the addressed register.

R/W = '0' sets a write operation and the data are written to the specified register.

R/W = '1' sets a read-back operation. Bits A4 to A0 select the register to be read. The remaining are don't care bits. During the next SPI operation, the data appearing on SDO pin are from the previously addressed register.

[A4:A0]—Address bits that specify which register is accessed.

DATA—16 data bits

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Table 6. Register Map

DATA BUS					DATA BITS													REGISTER
A4	A3	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3:D0	
0	0	0	0	0	A/B	LD	RST	PD-A	PD-B	SCE	X	GAIN-A	GAIN-B	DSDO	NOP	W2	X(1)	Configuration Register
0	0	0	0	1	Analog Monitor Select												X(1)	Monitor Register
0	0	0	1	0	GPIO-2	GPIO-1	GPIO-0	X(1)										GPIO Register
0	0	0	1	1	DB15:DB0(2)													Offset DAC-A Data
0	0	1	0	0	DB15:DB0(2)													Offset DAC-B Data
0	0	1	0	1	Reserved(3)													Reserved
0	0	1	1	0	SLEEP	Reserved(3)												SPI MODE
0	0	1	1	1	Reserved(3)													Reserved
0	1	0	0	0	DB15:DB0													DAC-0
0	1	0	0	1	DB15:DB0													DAC-1
0	1	0	1	0	DB15:DB0													DAC-2
0	1	0	1	1	DB15:DB0													DAC-3
0	1	1	0	0	DB15:DB0													DAC-4
0	1	1	0	1	DB15:DB0													DAC-5
0	1	1	1	0	DB15:DB0													DAC-6
0	1	1	1	1	DB15:DB0													DAC-7
1	0	0	0	0	DB15:DB0, default = 0 (0000h), twos complement													Zero Register-0
1	1	0	0	0	DB15:DB0, default = 32768 (8000h), straight binary													Gain Register-0
1	0	0	0	1	DB15:DB0, default = 0 (0000h), twos complement													Zero Register-1
1	1	0	0	1	DB15:DB0, default = 32768 (8000h), straight binary													Gain Register-1
1	0	0	1	0	DB15:DB0, default = 0 (0000h), twos complement													Zero Register-2
1	1	0	1	0	DB15:DB0, default = 32768 (8000h), straight binary													Gain Register-2
1	0	0	1	1	DB15:DB0, default = 0 (0000h), twos complement													Zero Register-3
1	1	0	1	1	DB15:DB0, default = 32768 (8000h), straight binary													Gain Register-3
1	0	1	0	0	DB15:DB0, default = 0 (0000h), twos complement													Zero Register-4
1	1	1	0	0	DB15:DB0, default = 32768 (8000h), straight binary													Gain Register-4
1	0	1	0	1	DB15:DB0, default = 0 (0000h), twos complement													Zero Register-5
1	1	1	0	1	DB15:DB0, default = 32768 (8000h), straight binary													Gain Register-5
1	0	1	1	0	DB15:DB0, default = 0 (0000h), twos complement													Zero Register-6
1	1	1	1	0	DB15:DB0, default = 32768 (8000h), straight binary													Gain Register-6
1	0	1	1	1	DB15:DB0, default = 0 (0000h), twos complement													Zero Register-7
1	1	1	1	1	DB15:DB0, default = 32768 (8000h), straight binary													Gain Register-7

(1) X = don't care—writing to this bit has no effect; reading the bit returns '0'.
(2) Table 3 lists the default values for a dual power supply. Offset DAC A and Offset DAC B are trimmed in manufacturing to minimize the error for symmetrical output. The default value may vary no more than ±10 LSB from the nominal number listed in Table 3. For a single power supply, the Offset DACs are turned off.
(3) Writing to a reserved bit has no effect; reading the bit returns '0'.

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INTERNAL REGISTERS

The DAC8718 internal registers consist of the Coinfiguration Register, the Monitor Register, the DAC Input Data Registers, the Zero Registers, the DAC Data Registers, and the Gain Registers, and are described in the following section.

The Configuration Register specifies which actions are performed by the device. Table 7 shows the details.

Table 7. Configuration Register (Default = 0000h)

BIT	NAME	DEFAULT VALUE	DESCRIPTION
D15	A/B	0	A/B bit. When A/B = '0', reading DAC-x returns the value in the Input Data Register. When A/B = '1', reading DAC-x returns the value in the DAC Data Register. When the correction engine is turned off, the data returned from the Input Data and DAC Data registers is the same. However, when the correction enngine is enabled, the data returned from the Input Data Register is the original data read from the bus, and the value in the DAC Data Register is the corrected data.
D14	LD	0	Synchronously update DACs bit. When $\overline{\text{LDAC}}$ is tied high, setting LD = '1' at any time after the write operation and the correction process complete synchronously updates all DAC latches with the content of the corresponding DAC Data Register, and sets V_{OUT} to a new level. The DAC8718 updates the DAC latch only if it has been accessed since the last time $\overline{\text{LDAC}}$ was brought low or the LD bit was set to '1', thereby eliminating unnecessary glitch. Any DACs that were not accessed are not reloaded. After updating, the bit returns to '0'. When the correction engine is turned off, bit LD can be set to '1' any time after the writing operation is complete; the DAC latch is immediately updated when bit LD is set. When the $\overline{\text{LDAC}}$ pin is tied low, this bit is ignored.
D13	RST	0	Software reset bit. Set the RST bit to '1' to reset the device; functions the same as a hardware reset. After reset completes, the RST bit returns to '0'.
D12	PD-A	0	Power-down bit for Group A. Setting the PD-A bit to '1' places Group A (DAC-0, DAC-1, DAC-2, and DAC-3) into power-down operation. All output buffers are in H-Z and all analog outputs (V_{OUT}-X) connect to SGND through an internal 15-kΩ resistor. The interface is still active. Setting the PD-A bit to '0' returns group A to normal operation.
D11	PD-B	0	Power-down bit for Group B. Setting the PD-B bit to '1' places Group B (DAC-4, DAC-5, DAC-6, and DAC-7) into power-down operation. All output buffers are in H-Z and all analog outputs (V_{OUT}-X) connect to SGND through an internal 15-kΩ resistor. The interface is still active. Setting the PD-B bit to '0' returns group B to normal operation.
D10	SCE	0	System-calibration enable bit. Set the SCE bit to '1' to enable the correction engine. When the engine is enabled, the input data are adjusted by the correction engine according to the contents of the corresponding Gain Register and Zero Register. The results are transferred to the corresponding DAC Data Register, and finally loaded into the DAC latch, which sets the V_{OUT}-x pin output level. Set the SCE bit to '0' to turn off the correction engine. When the engine is turned off, the input data are transferred to the corresponding DAC Data Register immediately after writing to the Input Data Register, and then loaded into the DAC latch, which sets the output voltage. Refer to the *User Calibration for Zero-Code Error and Gain Error* section for details.
D9	—	0	Reserved. Writing to this bit has no effect; reading this bit returns '0'.
D8	GAIN-A	1	Gain bit for Group A (DAC-0, DAC-1, DAC-2, and DAC-3). Set the GAIN-A bit to '0' for an output span = 6 × REF-A. Set the GAIN-A bit to '1' for an output span = 4 × REF-A.
D7	GAIN-B	0	Gain bit for Group B (DAC-4, DAC-5, DAC-6, and DAC-7). Set the GAIN-B bit to '0' for an output span = 6 × REF-A. Set the GAIN-B bit to '1' for an output span = 4 × REF-A.
D6	DSDO	0	Disable SDO bit. Set the DSDO bit to '0' to enable the SDO pin (default). The SDO pin works as a normal SPI output. Set the DSDO bit to '1' to disable the SDO pin. The SDO pin is always in a Hi-Z state no matter what the status of the $\overline{\text{CS}}$ pin is.
D5	NOP	1	No operation bit. During a write operation, setting the NOP bit to '1' has no effect (the bit returns to '0' when the write operation completes). Setting the NOP bit to '0', returns the device to normal operation. During a read operation, the bit always returns “0”
D4	W2	1	Second wake-up operation bit. If the $\overline{\text{WAKEUP}}$ pin is high, an alternative method to wake-up the device from sleep in SPI is by using the $\overline{\text{CS}}$ pin. When W2 = '1', the rising edge of $\overline{\text{CS}}$ restores the device from sleep mode to normal operation, if no more than one falling edge of SCLK exists while $\overline{\text{CS}}$ is low. However, the device will not wake up if more than one falling edge of SCLK exists. Setting the W2 bit to '0' disables this function, and the rising edge of $\overline{\text{CS}}$ does not wake up the device. If the $\overline{\text{WAKEUP}}$ is low, this bit is ignored and the device is always in normal mode.
D3:D0	—	0	Reserved. Writing to these bits has no effect; reading these bits returns '0'.

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Monitor Register (default = 0000h).

The Monitor Register selects which DAC-n, reference buffer outputs, Offset DACs, or external signals (AIN-0 and AIN-1) are to be monitored by the V_{MON} pin. Only one bit at a time can be set to '1'. When all bits = '0', the monitor is disabled and V_{MON} is in a Hi-Z state.

Table 8. Monitor Register (Default = 0000h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3:D0	V_{MON} CONNECTS TO
0	0	0	0	0	0	0	0	0	0	0	1	X(1)	Reference buffer B output
0	0	0	0	0	0	0	0	0	0	1	0	X	Reference buffer A output
0	0	0	0	0	0	0	0	0	1	0	1	X	Offset DAC B output
0	0	0	0	0	0	0	0	0	1	1	0	X	Offset DAC A output
0	0	0	0	0	0	0	0	0	1	0	0	X	AIN-0
0	0	0	0	0	0	0	0	1	0	0	0	X	AIN-1
0	0	0	0	0	0	0	1	0	0	0	0	X	DAC-0
0	0	0	0	0	0	1	0	0	0	0	0	X	DAC-1
0	0	0	0	0	1	0	0	0	0	0	0	X	DAC-2
0	0	0	0	1	0	0	0	0	0	0	0	X	DAC-4
0	0	0	1	0	0	0	0	0	0	0	0	X	DAC-4
0	0	1	0	0	0	0	0	0	0	0	0	X	DAC-5
0	1	0	0	0	0	0	0	0	0	0	0	X	DAC-6
1	0	0	0	0	0	0	0	0	0	0	0	X	DAC-7
0	0	0	0	0	0	0	0	0	0	0	0	X	Monitor function disabled, Hi-Z (default)

(1) X = don't care.

GPIO Register. Default = E000h.

The GPIO Register determines the status of each GPIO pin.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
GPIO-2	GPIO-1	GPIO-0	X	X	X	X	X	X	X	X	X	X	X	X	X

GPIO-2:0

For write operations, the GPIO-n pin operates as an output. Writing a '1' to the GPIO-n bit sets the GPIO-n pin to high impedance, and writing a '0' sets the GPIO-n pin to logic low. An external pull-up resistor is required when using the GPIO-n pin as an output.

For read operations, the GPIO-n pin operates as an input. Read the GPIO-n bit to receive the status of the corresponding GPIO-n pin. Reading a '0' indicates that the GPIO-n pin is low, and reading a '1' indicates that the GPIO-n pin is high.

After power-on reset, or any forced hardware or software reset, all GPIO-n bits are set to '1', and are in a high impedance state.

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SPI MODE Register. Default = 0000h.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SLEEP	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

SLEEP

Set the SLEEP bit to '1' to put the device into SPI sleep mode.

When the SLEEP bit = '0', the SPI is in normal mode. The bit is cleared ('0') after a hardware reset (through the $\overline{\text{RST}}$ pin) or if the $\overline{\text{WAKEUP}}$ pin is low.

For normal SPI operation, the data entering the SDI pin is transferred into the Shift Register. However, for SPI sleep mode, the Shift Register is bypassed. The data entering into the SDI pin are directly transferred to the SDO pin instead of the Shift Register.

APPLICATION INFORMATION

POWER-SUPPLY DECOUPLING

The DAC8718 should have supply decoupling of 10 μF in parallel with 0.1 μF on each supply, located as close to the package as possible; ideally right up against the device. The 10-μF capacitors are tantalum-bead type. The 0.1-μF capacitor should have low effective series resistance (ESR) and low effective series inductance (ESI), such as ceramic types that provide a low impedance path to ground at high frequencies in order to handle transient currents due to internal logic switching.

LAYOUT

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout can help to improve performance. The printed circuit boards on which the DAC8718 are mounted should be designed so that the analog and digital sections are separated and confined to certain areas of the board. If the DAC8718 are in a system where multiple devices require an AGND-to-DGND connection, the connection should be made at one point only. The star ground point should be established as close as possible to the device. For supplies with multiple pins, it is recommended that these pins be tied together and that each supply be decoupled only once.

Digital lines running under the device should be avoided because they can couple noise onto the device. The analog ground plane should be allowed to run under the DAC8718 to avoid noise coupling. The power supply lines should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching digital signals should be shielded with digital ground to avoid radiating noise to other parts of the board, and they should never be run near the reference inputs. It is essential to minimize noise on the REF-A and REF-B lines.

Avoid crossover of digital and analog signals. Traces on oppo-site sides of the board should run at right angles to each other. This reduces the effects of feedthrough across the board.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
DAC8718SPAG	PREVIEW	TQFP	PAG	64	160	TBD	Call TI	Call TI
DAC8718SPAGR	PREVIEW	TQFP	PAG	64	1500	TBD	Call TI	Call TI
DAC8718SRGZR	PREVIEW	QFN	RGZ	48	2500	TBD	Call TI	Call TI
DAC8718SRGZT	PREVIEW	QFN	RGZ	48	250	TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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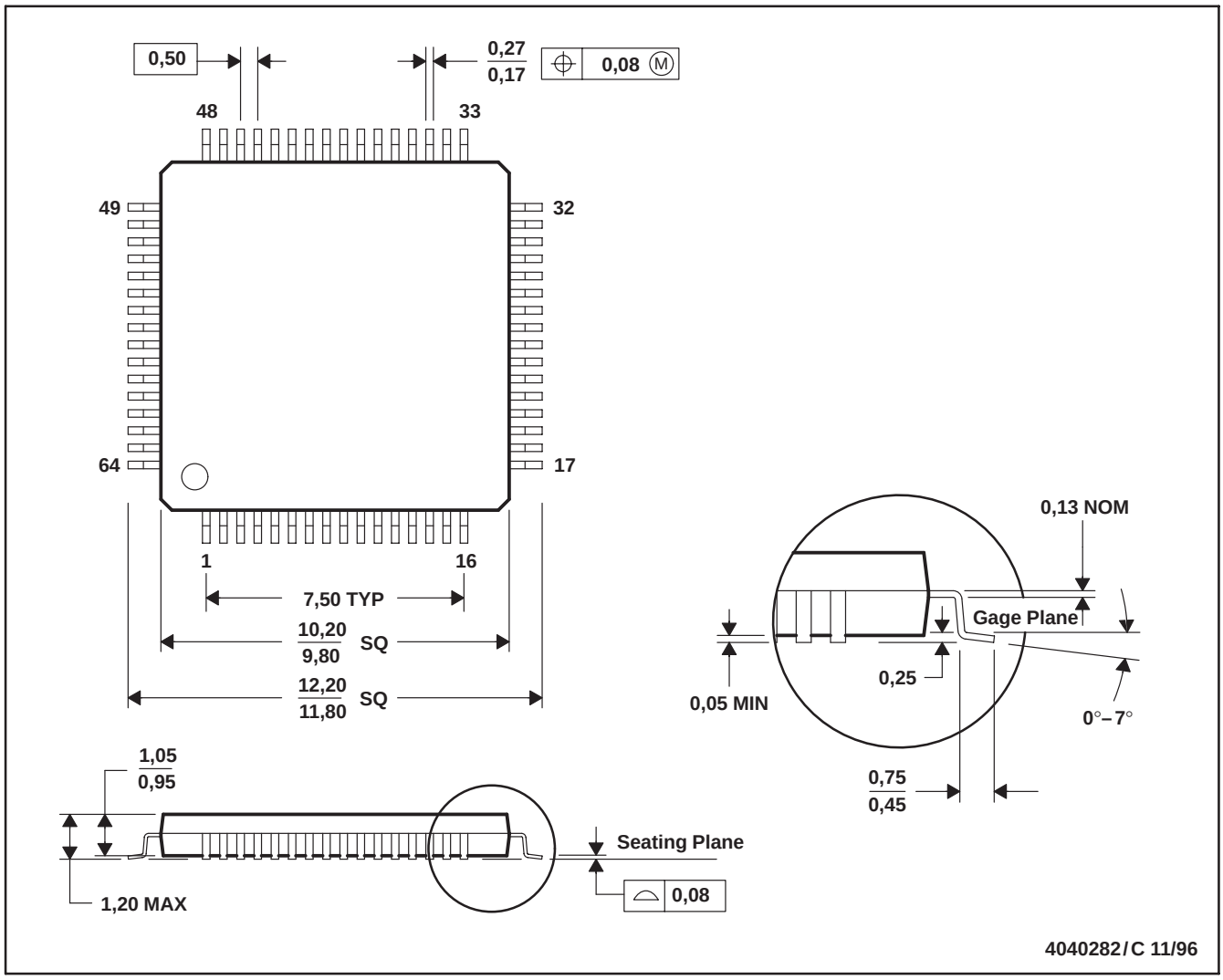
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

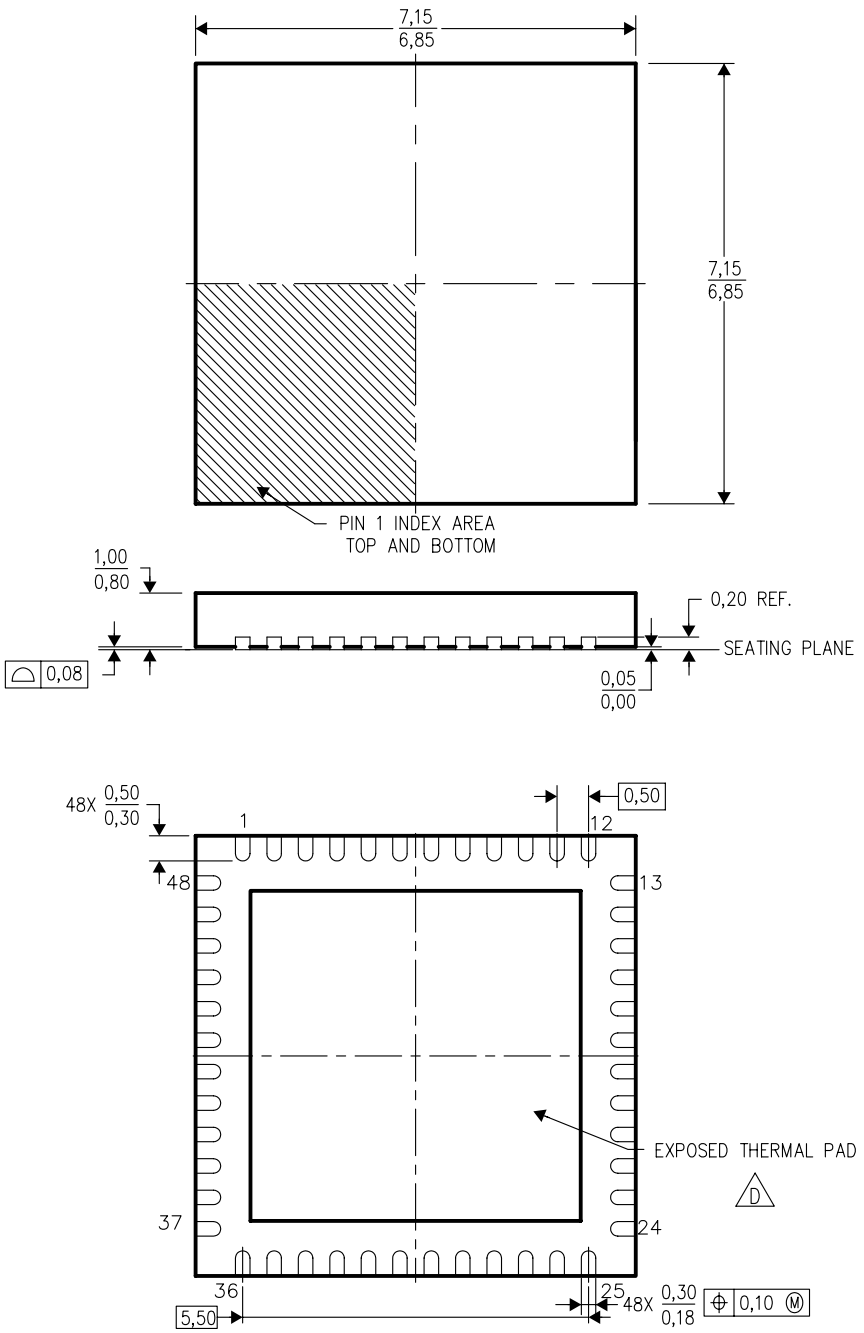
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

PAG (S-PQFP-G64) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

RGZ (S–PQFP–N48) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

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