IXYS

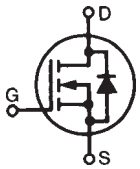
Trench Gate Power MOSFET

IXTQ88N28T

V_{DSS} = 280V
I_{D25} = 88A
$R_{DS(on)}$ ≤ 44mΩ

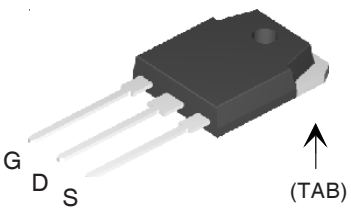
N-Channel Enhancement Mode

For Plasma Display Applications



Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	T_J = 25°C to 150°C	280	V
V_{DGR}	T_J = 25°C to 150°C; R_{GS} = 1 MΩ	280	V
V_{GSM}	Transient	±30	V
I_{D25}	T_C = 25°C	88	A
I_{DRMS}	External lead current limit	75	A
I_{DM}	T_C = 25°C, pulse width limited by T_{JM}	250	A
P_D	T_C = 25°C	625	W
T_J		-55 ... +150	°C
T_{JM}		150	°C
T_{stg}		-55 ... +150	°C
T_L	Maximum lead temperature for soldering	300	°C
T_{SOLD}	1.6mm (0.062 in.) from case for 10s	260	°C
M_d	Mounting torque	1.13/10	Nm/lb.in.
Weight		5.5	g

TO-3P (IXTQ)



G = Gate D = Drain
S = Source TAB = Drain

Features

- Trench gate construction for low $R_{DS(on)}$
- International standard package
- Low package inductance
  - easy to drive and to protect

Advantages

- Easy to mount
- Space savings

Symbol (T_J = 25°C, unless otherwise specified)	Test Conditions	Characteristic Values Min.	Typ.	Max.	
V_{DSS}	V_{GS} = 0 V, I_D =1mA	280			V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 1mA	3.0		5.0	V
I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0V			±200	nA
I_{DSS}	$V_{DS} = V_{DSS}$, V_{GS} = 0 V			1	μA
	$V_{DS} = V_{DSS}$, V_{GS} = 0 V, T_J = 125°C			200	μA
$R_{DS(on)}$	V_{GS} = 10 V, $I_D = 0.5 \bullet I_{D25}$, Note1		38	44	mΩ

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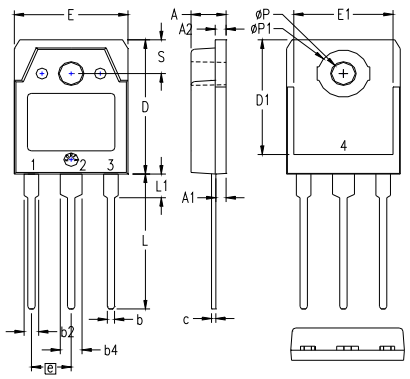
Symbol	Test Conditions	Characteristic Values (T_J = 25°C, unless otherwise specified) Min.	Typ.	Max.	
g_{fs}	V_{DS}= 10 V, I_D = 0.5 I_{D25}, Note 1	40	66		S
C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		5750		pF
C_{oss}			600		pF
C_{rss}			52		pF
$t_{d(on)}$	**Resistive Switching Times**		38		ns
t_r	V_{GS} = 15 V, V_{DS} = 220 V, I_D = 44A		60		ns
$t_{d(off)}$	R_G = 5Ω (External)		96		ns
t_f			57		ns
$Q_{g(on)}$	V_{GS}= 10 V, V_{DS} = 0.5 • V_{DSS}, I_D = 0.5 • I_{D25}		138		nC
Q_{gs}			48		nC
Q_{gd}			40		nC
R_{thJC}				0.20	°C/W
R_{thCK}			0.25		°C/W

Source-Drain Diode

Symbol	Test Conditions (T_J = 25°C, unless otherwise specified)	Characteristic Values Min.	typ.	Max.	
I_S	V_{GS} = 0 V			88	A
I_{SM}	Repetitive, pulse width limited by T_{JM}			250	A
V_{SD}	I_F = I_S, V_{GS} = 0 V, Note 1			1.5	V
t_{rr}	I_F = 25 A, -di/dt = 100 A/μs		200		ns
Q_{RM}	V_R = 100 V		2.0		μC

Notes: 1. Pulse test, t ≤ 300μs; duty cycle, d ≤ 2%.

TO-3P (IXTQ) Outline



1 – GATE
2 – DRAIN (COLLECTOR)
3 – SOURCE (EMITTER)
4 – DRAIN (COLLECTOR)

SYM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.185	.193	4.70	4.90
A1	.051	.059	1.30	1.50
A2	.057	.065	1.45	1.65
b	.035	.045	0.90	1.15
b2	.075	.087	1.90	2.20
b4	.114	.126	2.90	3.20
c	.022	.031	0.55	0.80
D	.780	.791	19.80	20.10
D1	.665	.677	16.90	17.20
E	.610	.622	15.50	15.80
E1	.531	.539	13.50	13.70
e	.215 BSC		5.45 BSC	
L	.779	.795	19.80	20.20
L1	.134	.142	3.40	3.60
øP	.126	.134	3.20	3.40
øP1	.272	.280	6.90	7.10
S	.193	.201	4.90	5.10

All metal area are tin plated.

IXYS reserves the right to change limits, test conditions, and dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents: 4,835,592 4,850,072 4,881,106 4,931,844 5,017,508 5,034,796 5,049,961 5,063,307 5,187,117 5,237,481 5,381,025 5,486,715 6,162,665 6,259,123B1 6,306,728B1 6,404,065B1 6,534,343 6,583,505 6,683,344 6,710,405B2 6,710,463 6,727,585 6,759,692 6,771,478B2 7,005,734B2 7,063,975B2 7,071,537 7,157,338B2

Fig. 1. Output Characteristics @ 25°C

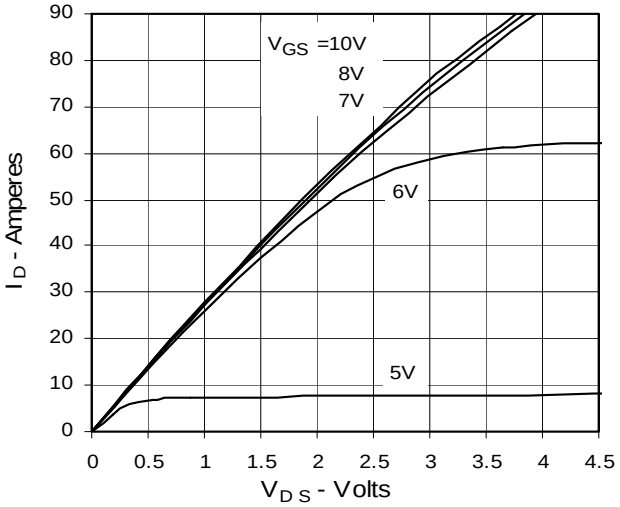


Fig. 2. Extended Output Characteristics @ 25°C

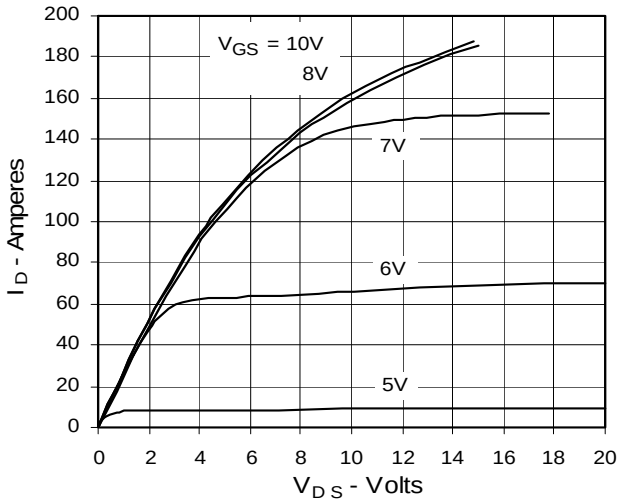


Fig. 3. Output Characteristics @ 125°C

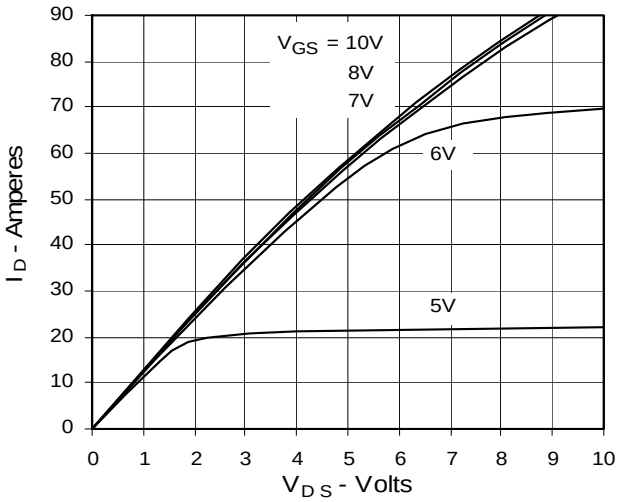


Fig. 4. $R_{DS(on)}$ Normalized to 0.5 I_{D25} Value vs. Junction Temperature

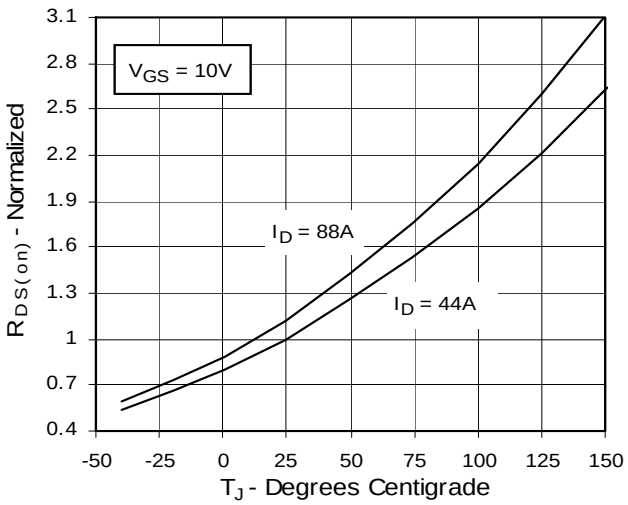


Fig. 5. $R_{DS(on)}$ Normalized to 0.5 I_{D25} Value vs. I_D

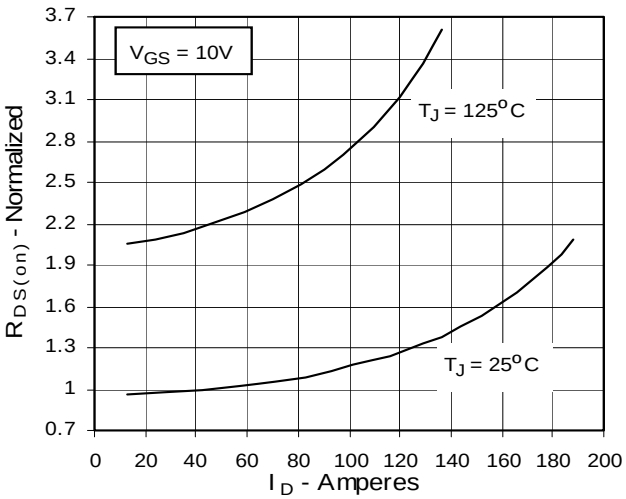
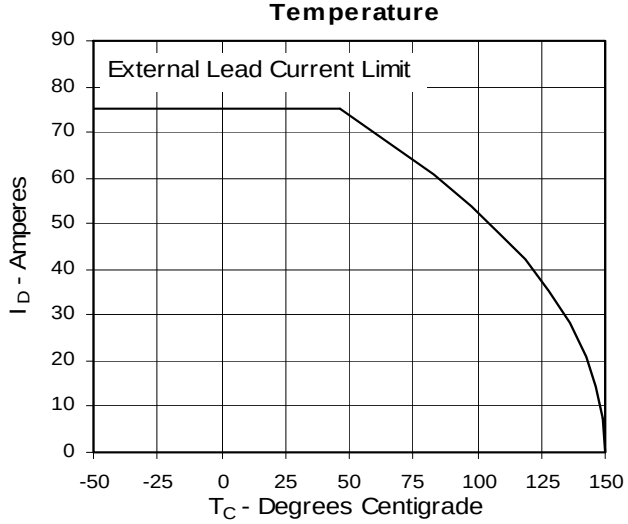


Fig. 6. Drain Current vs. Case Temperature



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Fig. 7. Input Admittance

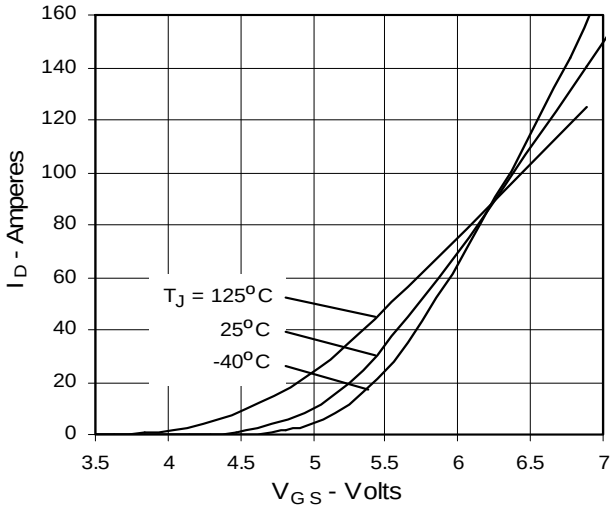


Fig. 8. Transconductance

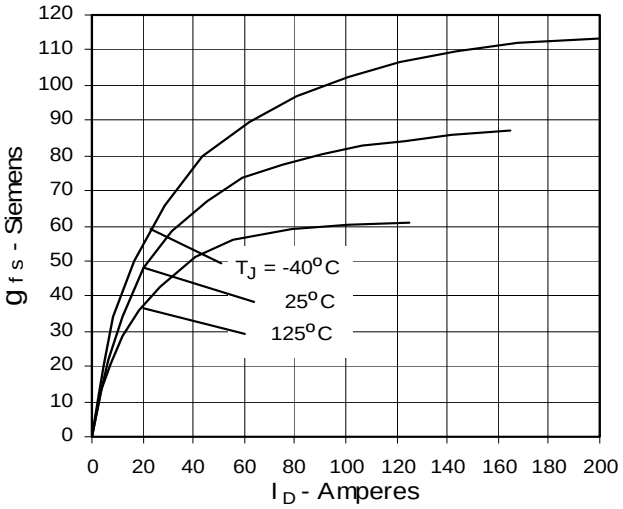


Fig. 9. Source Current vs. Source-To-Drain Voltage

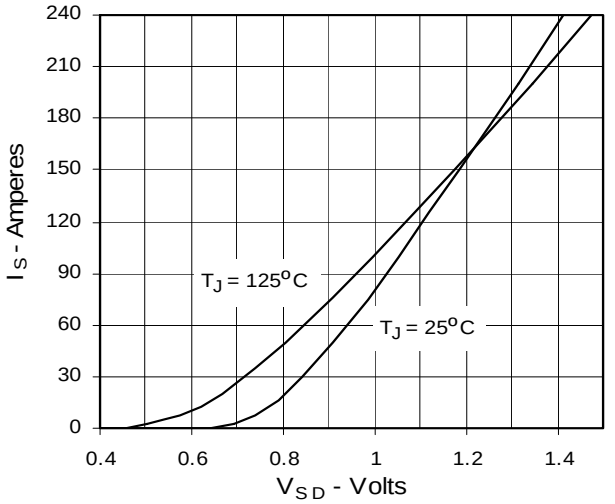


Fig. 10. Gate Charge

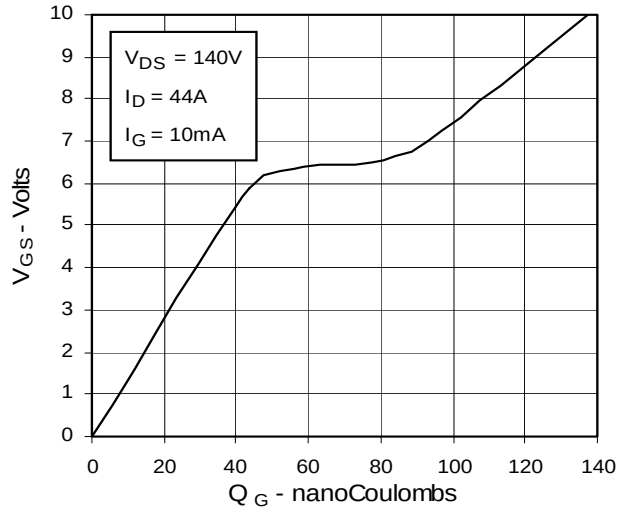


Fig. 11. Capacitance

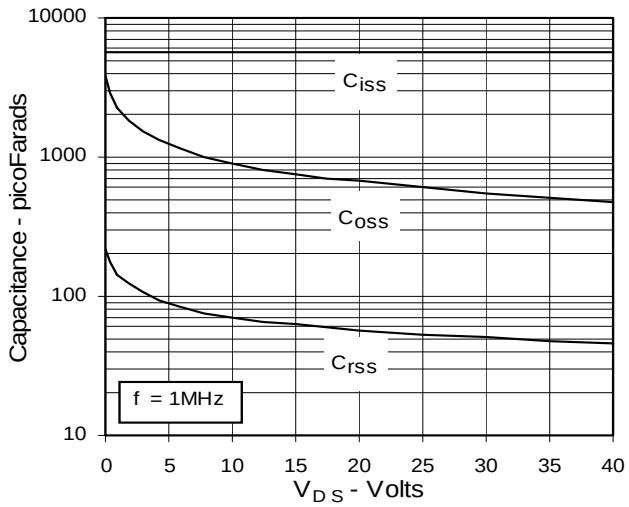
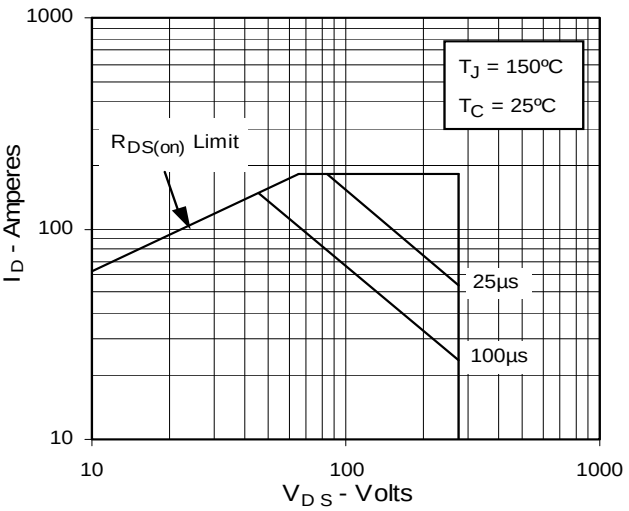
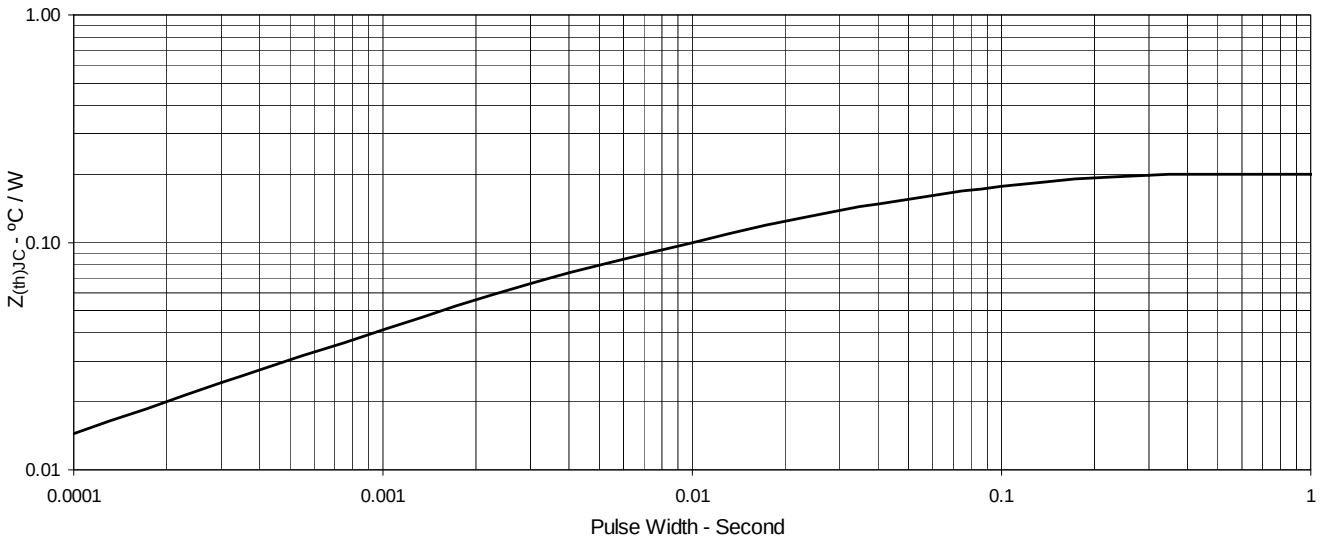


Fig. 12. Forward-Bias Safe Operating Area



I> sions.

Fig. 13. Maximum Transient Thermal Impedance



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