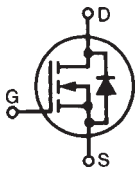
IXYS

Preliminary Technical Information

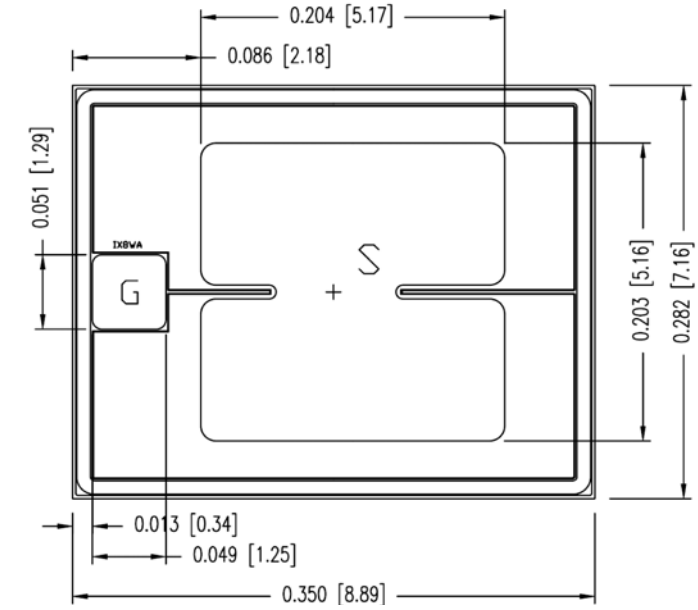
IXTD110N25T-8W V_{DSS} = 250V

Trench Gate Power MOSFET Die

N-Channel Enhancement Mode



Die Outline



Dimensions in inches [mm}

Notes:

1. Die Thickness: 200 ± 25 μm
2. Die Size Tolerance: ± 50 μm
3. Top Bonding Pad Metal: 30 KÅ nominally thick Al
4. Back Metal: 3 layers of Ti, Ni & Au; 2500Å nominally thick Au
5. G = Gate, S = Source D = Drain (back side)
6. Recommend wire bonding: Gate: 1 x 200 μm diameter Al wire Source: 4 x 300 μm diameter Al wire
7. ESD sensitivity: Class 1C per JEDEC Standard No. 22-A114-B
8. Dice are visually inspected per IXYS Assembly Specification AS0011.

Symbol	Test Conditions [1]	Maximum Ratings	
V_{DSS}	T_J = 25°C to 150°C	250	V
V_{GSM}		±30	V
I_{D25}	T_C = 25°C	110	A
T_{JM}		150	°C

Symbol	Test Conditions (T_J = 25°C, unless otherwise specified)	Characteristic Values Min.	Typ.	Max.	
BV_{DSS}	V_{GS} = 0V, I_D = 250μA, Note 1	250			V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 1 mA, Note 1	2.5		4.5	V
I_{GSS}	V_{GS} = ±20V, V_{DS} = 0V, Note 1			±200	nA
I_{DSS}	$V_{DS} = V_{DSS}$, V_{GS} = 0V, Note 1			5	μA
$R_{DS(on)}$	V_{GS} = 10V, $I_D = 0.5 \bullet I_{D25}$, Note 2 & 4			24	mΩ

Symbol	Test Conditions[2] (T_J = 25°C, unless otherwise specified)	Characteristic Values[3] Min.	Typ.	Max.	
g_{fs}	V_{DS}= 10V, I_D = 0.5 • I_{D25}, Note 4		65	110	S
C_{iss}	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz		9400		pF
C_{oss}			851		pF
C_{rss}			55		pF
$t_{d(on)}$	**Resistive Switching Times**		19		ns
t_r	V_{GS} = 15V, V_{DS} =0.5 • V_{DSS}, I_D = 0.5 • I_{D25}		27		ns
$t_{d(off)}$	R_G = 2Ω (External)		60		ns
t_f			27		ns
$Q_{g(on)}$	V_{GS}= 10V, V_{DS} = 0.5 • V_{DSS}, I_D = 25A		157		nC
Q_{gs}			40		nC
Q_{gd}			50		nC

Source-Drain Diode

Symbol	Test Conditions[2] (T_J = 25 °C, unless otherwise specified)	Characteristic Values[2] Min.	Typ.	Max.	
I_S	V_{GS} = 0V			110	A
I_{SM}	Repetitive, pulse width limited by T_{JM}			350	A
V_{SD}	I_F = 55A, V_{GS} = 0V,			1.2	V
T_{rr}	I_F = 55A, -di/dt = 250 A/μs V_R = 100 V		170		ns
Q_{RM}			2.3		μC
I_{RM}			27		A

Notes:

1. Tested 100% on wafer.
2. Not tested at the wafer level. Die must be properly attached to a suitable substrate, e.g. copper lead frame, in order to measure $R_{DS(on)}$.
3. The curves attached to this Data Sheet were derived using this die in the IXTH110N25T Trench Gate MOSFET package.
4. Pulse test, t ≤ 300 μs, duty cycle, d ≤ 2 %.

PRELIMINARY TECHNICAL INFORMATION

The product presented herein is under development. The Technical Specifications offered are derived from data gathered during objective characterizations of preliminary engineering lots; but also may yet contain some information supplied during a pre-production design evaluation. IXYS reserves the right to change limits, test conditions, and dimensions without notice.

Fig. 1. Output Characteristics @ 25ºC

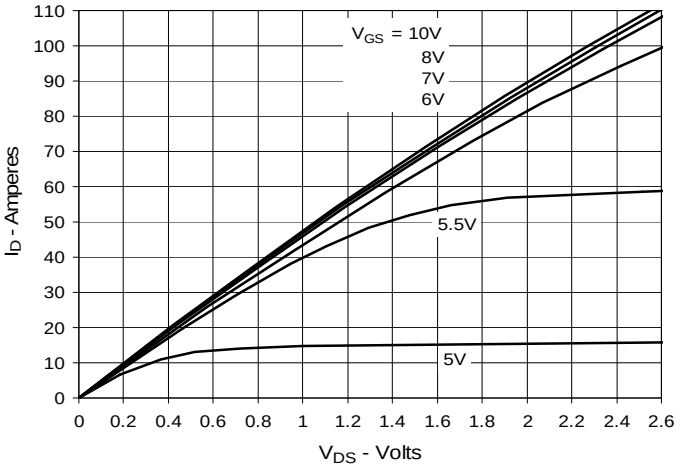


Fig. 2. Extended Output Characteristics @ 25ºC

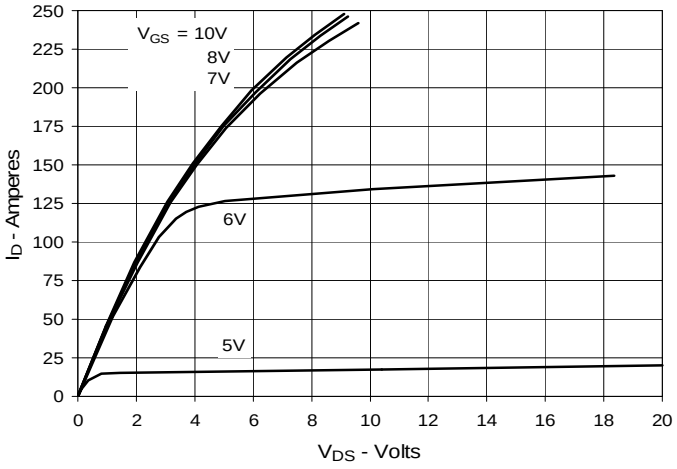


Fig. 3. Output Characteristics @ 125ºC

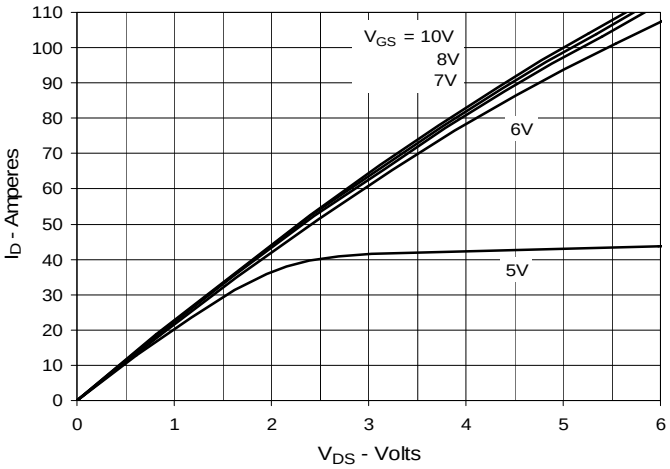


Fig. 4. $R_{DS(on)}$ Normalized to I_D = 55A Value vs. Junction Temperature

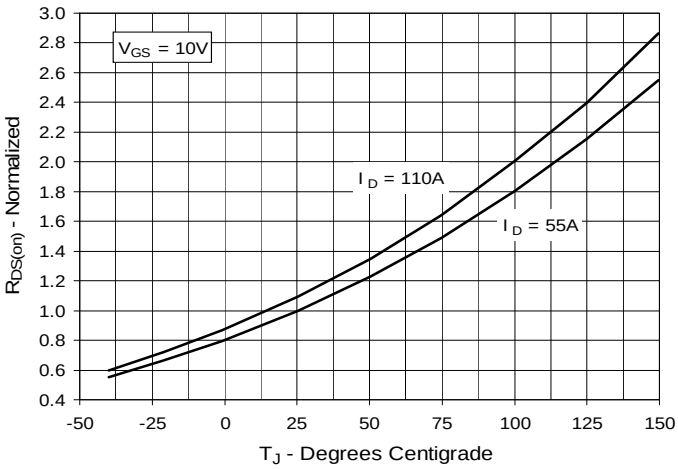


Fig. 5. $R_{DS(on)}$ Normalized to I_D = 55A Value vs. Drain Current

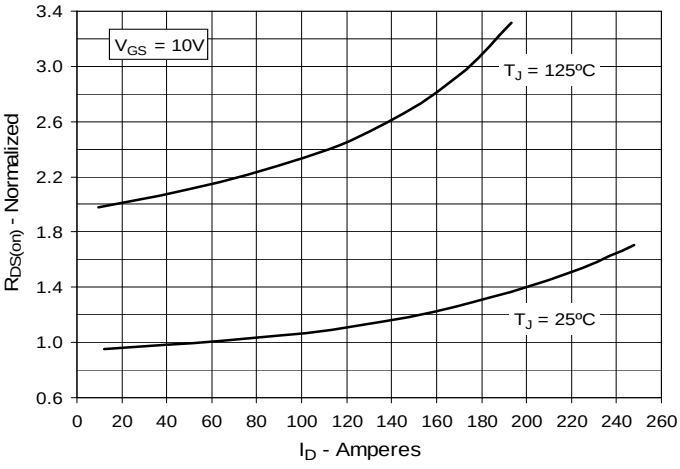


Fig. 6. Maximum Drain Current vs. Case Temperature

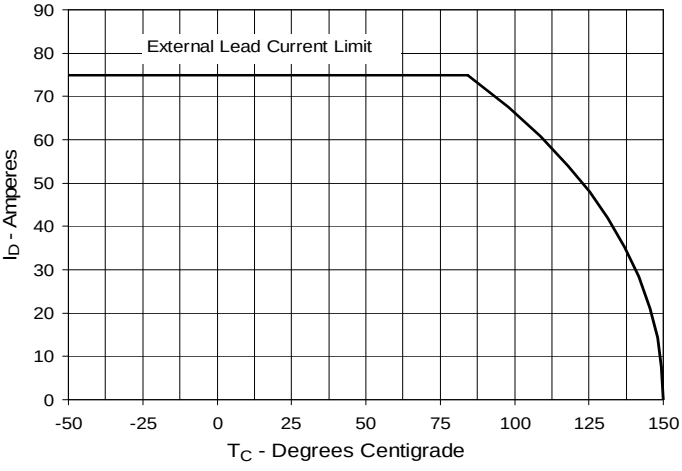


Fig. 7. Input Admittance

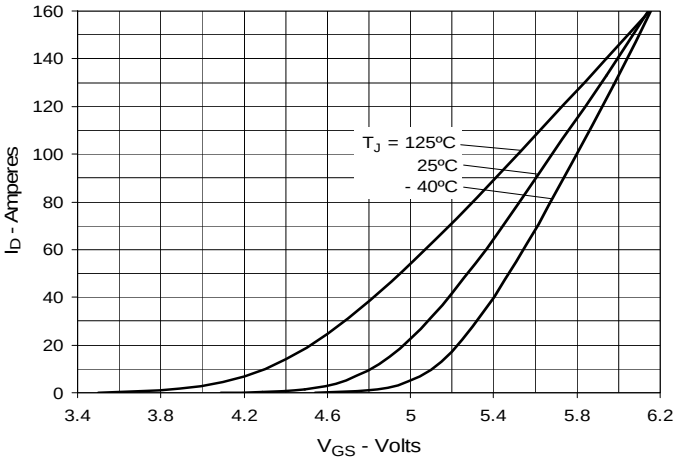


Fig. 8. Transconductance

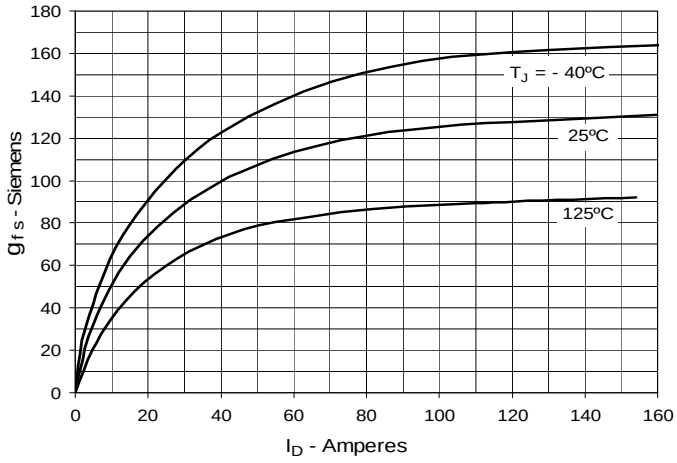


Fig. 9. Forward Voltage Drop of Intrinsic Diode

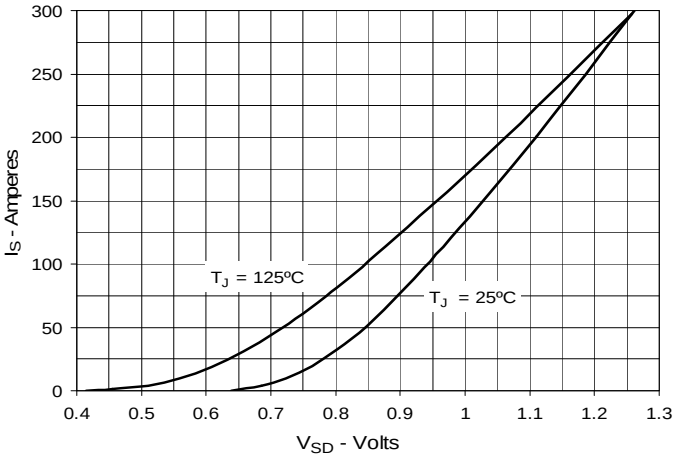


Fig. 10. Gate Charge

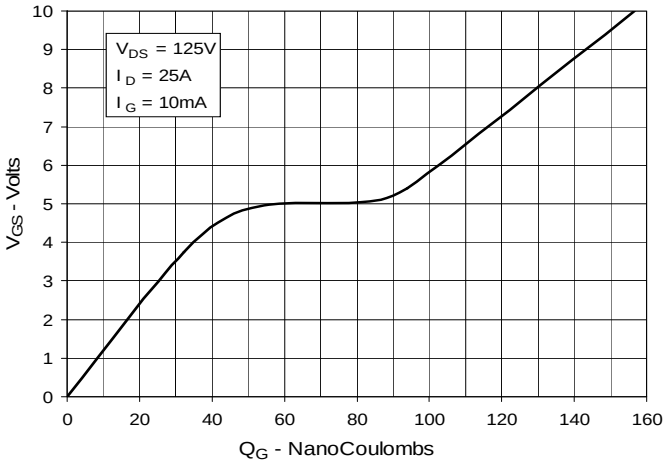


Fig. 11. Capacitance

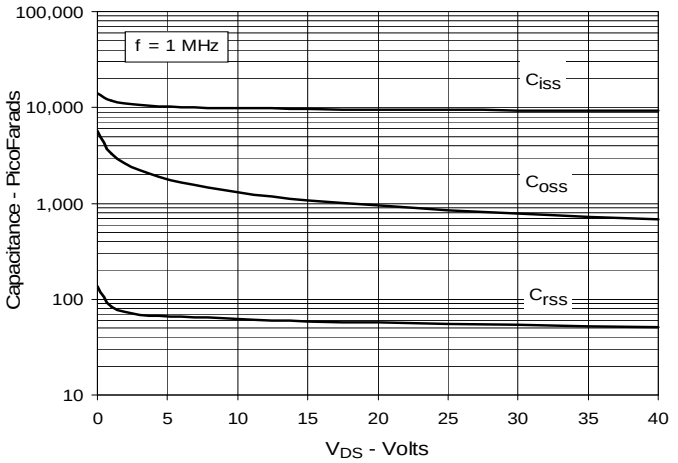


Fig. 12. Resistive Turn-on Rise Time vs. Junction Temperature

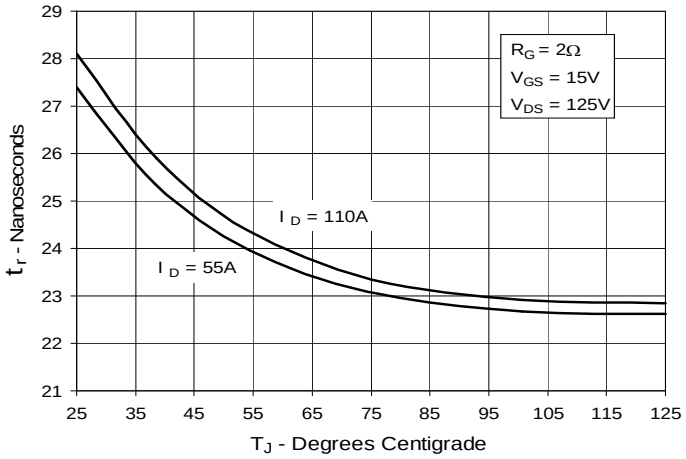


Fig. 13. Resistive Turn-on Rise Time vs. Drain Current

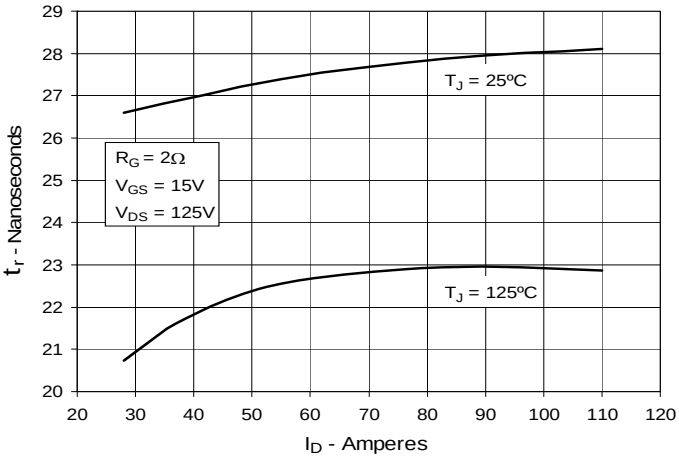


Fig. 14. Resistive Turn-on Switching Times vs. Gate Resistance

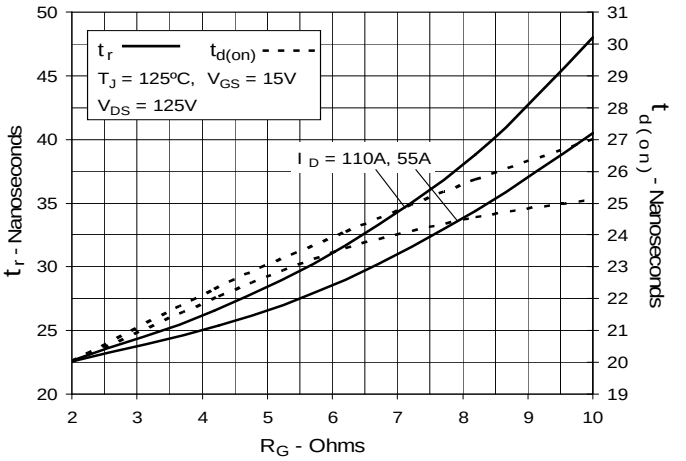


Fig. 15. Resistive Turn-off Switching Times vs. Junction Temperature

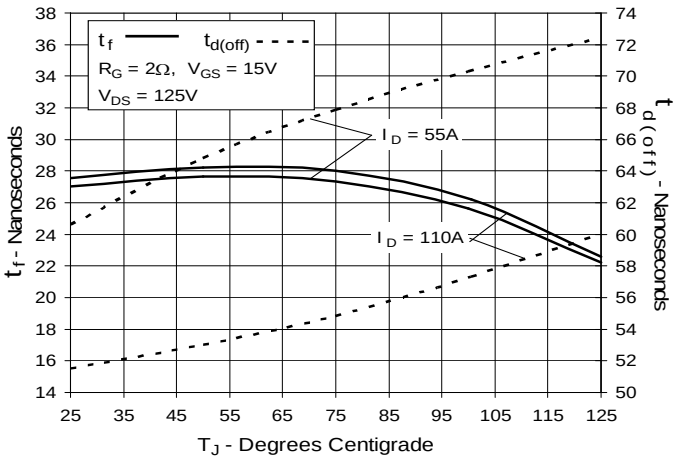


Fig. 16. Resistive Turn-off Switching Times vs. Drain Current

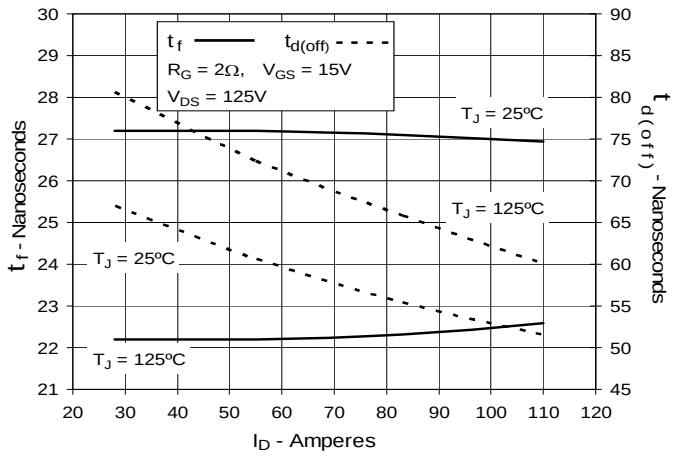


Fig. 17. Resistive Turn-off Switching Times vs. Gate Resistance