MGA-30116

750MHz – 1GHz

½ Watt High Linearity Amplifier

Data Sheet

Description

Avago Technologies' MGA-30116 is a high linearity ½ Watt PA with good OIP3 performance and exceptionally good PAE at p1dB gain compression point, achieved through the use of Avago Technologies' proprietary 0.25um GaAs Enhancement-mode pHEMT process.

The adjustable temperature compensated internal bias circuit allowed the device to be operated at either class A or class AB operation

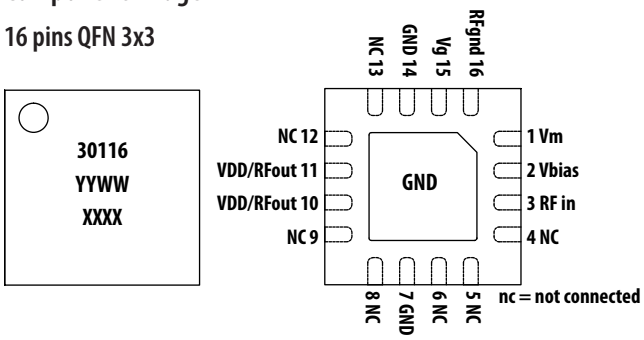
The MGA-30116 is housed inside a standard 16 pin QFN 3X3 package.

Applications

- Class A driver amplifier for GSM/CDMA Base Stations.
- General purpose gain block.

Component Image

16 pins QFN 3x3



TOP VIEW **BOTTOM VIEW**

Notes:
Package marking provides orientation and identification
"30116" = Device Part Number
"YYWW" = Work Week and Year of manufacture
"XXXX" = Last 4 digit of Lot number

Features

- High linearity and P1dB
- Built in adjustable temperature compensated internal bias circuitry
- GaAs E-pHEMT Technology [1]
- Standard QFN 3X3 package
- 5V supply
- Excellent uniformity in product specifications
- Tape-and-Reel packaging option available
- MSL-1 and Lead-free
- High MTTF for base station application

Specifications

900MHz; 5V, 202.8mA (typical)

- 17.0 dB Gain
- 44.1 dBm Output IP3
- 27.7 dBm Output Power at 1dB gain compression
- 47.0% PAE at P1dB
- 2.0 dB Noise Figure

Notes:
1. Enhancement mode technology employs positive gate voltage, thereby eliminating the need of negative gate voltage associated with conventional depletion mode devices.

Attention: Observe precautions for handling electrostatic sensitive devices.
ESD Machine Model = 60 V
ESD Human Body Model = 300 V
Refer to Avago Application Note A004R: *Electrostatic Discharge, Damage and Control.*

Absolute Maximum Rating [1] T_A=25°C

Symbol	Parameter	Units	Absolute Max.
$V_{dd,max}$	Device Voltage, RF output to ground	V	5.5
$I_{ds,max}$	Device Drain Current	mA	400
$V_{ctrl,max}$	Control Voltage	V	5.5
$P_{in,max}$	CW RF Input Power	dBm	22
P_{diss}	Total Power Dissipation [3]	W	2.2
$T_{j,\ max}$	Junction Temperature	°C	150
T_{STG}	Storage Temperature	°C	-65 to 150

Thermal Resistance [2] θ_{jc} = 33 °C/W (Vdd=5, Ids=200mA, Tc=85°C)

Notes:
1. Operation of this device in excess of any of these limits may cause permanent damage.
2. Thermal resistance measured using Infra-Red measurement technique.
3. This is limited by maximum Vdd and Ids. Derate 30.3mW/ °C for Tc> 77.5 °C.

Electrical Specifications [4]

T_A = 25°C, Vdd =5V, Vctrl =5V, RF performance at 900 MHz, measured on demo board (see Fig. 7) unless otherwise specified.

Symbol	Parameter and Test Condition	Units	Min.	Typ.	Max.
Ids	Quiescent current	mA	165	202.8	240
Ictrl	Vctrl current	mA	-	7	-
Gain	Gain	dB	15.5	17.0	18.5
OIP3 [5]	Output Third Order Intercept Point	dBm	41	44.1	-
OP1dB	Output Power at 1dB Gain Compression	dBm	26.2	27.7	-
PAE	Power Added Efficiency	%	-	47.0	-
NF	Noise Figure	dB	-	2.0	-
S11	Input Return Loss, 50Ω source	dB	-	-14	-
S22	Output Return Loss, 50Ω load	dB	-	-14	-
S12	Reverse Isolation	dB	-	-23.5	-

Notes:
4. Measurements at 900MHz obtained using demo board described in Figure 6 and 7.
5. 900 MHz OIP3 test condition: F_{RF1} - F_{RF2} = 10MHz with input power of -5dBm per tone measured at worse side band
6. Use proper biasing, heat sink and de-rating to ensure maximum channel temperature is not exceeded. See absolute maximum ratings and application note (if applicable) for more details.

Product Consistency Distribution Charts [1,2]

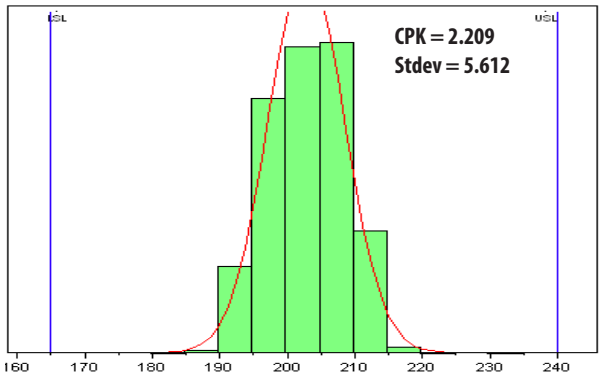


Figure 1. Ids at 900MHz; LSL=165mA, nominal =202.8mA, USL=240mA

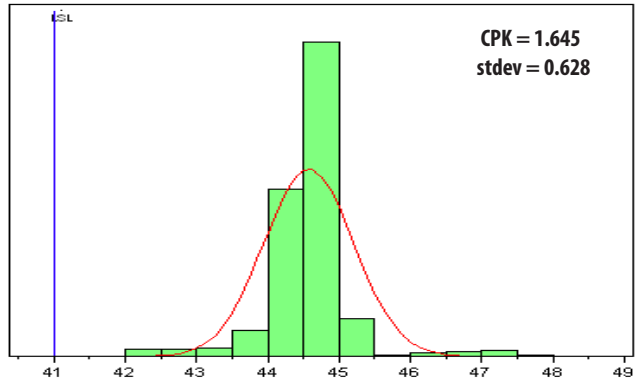


Figure 2. OIP3 at 900MHz; LSL=41dB, nominal=44.1dBm

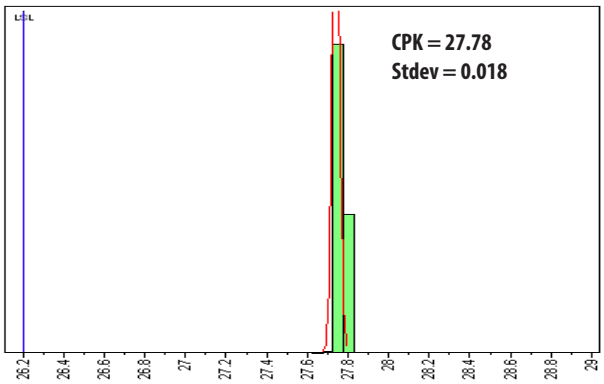


Figure 3. P1dB at 900MHz; LSL, 26.2dBm, nominal=27.7dBm

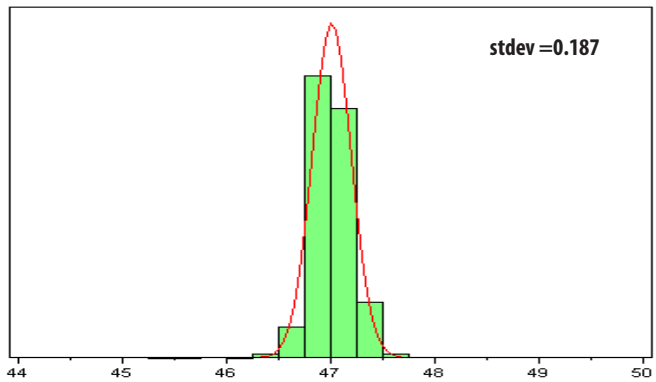


Figure 4. PAE at P1dB 900MHz; nominal=47.0%

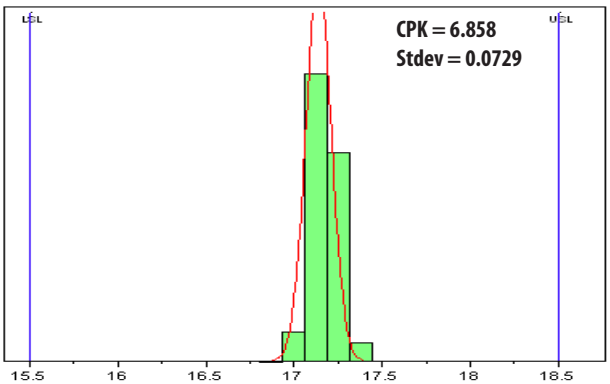


Figure 5. Gain at 900MHz; LSL=15.5dB, Nominal =17.0dB, USL=18.5dB,

Notes:

1. Distribution data sample size is 500 samples taken from 2 different wafer lots and 3 different wafers. Future wafers allocated to this product may have nominal values anywhere between the upper and lower limits.
2. Measurements were made on a characterization test board, which represents a trade-off between optimal OIP3, gain, P1dB and PAE. Circuit trace losses have not been de-embedded from measurements above.

S-Parameter (Vdd=5V, Vctrl=5V, T=25°C, unmatched 50 ohm)

Freq (GHz)	S11 (dB)	S11 (ang)	S21 (dB)	S21 (ang)	S12 (dB)	S12 (ang)	S22 (dB)	S22 (ang)
0.1	-10.29	-177.05	7.75	-106.14	-56.49	-170.86	-0.48	-158.78
0.2	-10.01	126.39	15	-105.81	-42.75	-179.05	-1.23	167.99
0.3	-8.18	55.14	21.39	-126.7	-34.06	168.62	-2.73	142.08
0.4	-4.26	-36.48	24.86	-175.06	-27.01	131.15	-11.71	108.03
0.5	-4.56	-98.84	22.89	143.15	-26.17	96.88	-11.34	-148.58
0.6	-3.94	-121.6	20.8	129.14	-25.69	88.03	-8.16	-162.17
0.7	-4.39	-142.07	19	115.84	-25.35	78.94	-6.65	-165.6
0.8	-4.79	-154.52	17.41	107.43	-25	73.93	-5.97	-169.46
0.9	-5	-163.57	16.09	101.39	-24.53	70.71	-5.62	-172.67
1	-5.28	-171.09	14.99	96.49	-24.05	68.2	-5.42	-175.13
1.1	-5.37	-176.68	14.13	92.83	-23.56	66.38	-5.32	-176.92
1.2	-5.52	177.46	13.27	89.06	-23.04	64.39	-5.24	-178.58
1.3	-5.57	172.69	12.54	85.8	-22.49	62.63	-5.21	-179.86
1.4	-5.67	167.94	11.87	82.7	-21.99	60.81	-5.19	179.08
1.5	-5.74	163.82	11.27	79.75	-21.48	59.04	-5.2	178.27
1.6	-5.87	159.69	10.7	76.99	-20.99	57.3	-5.23	177.52
1.7	-5.97	155.85	10.2	74.28	-20.51	55.48	-5.29	176.89
1.8	-6.12	152.03	9.77	72.01	-20.1	53.9	-5.37	176.17
1.9	-6.25	148.11	9.34	69.48	-19.64	52.08	-5.47	175.59
2	-6.39	143.46	8.92	66.86	-19.15	50.16	-5.59	174.76
2.1	-6.49	139.69	8.59	64.49	-18.76	48.34	-5.7	174.22
2.2	-6.59	135.32	8.26	61.98	-18.33	46.35	-5.84	173.48
2.3	-6.65	131.37	7.93	59.34	-17.92	44.15	-5.97	172.89
2.4	-6.72	127.15	7.63	56.78	-17.53	41.94	-6.13	172.15
2.5	-6.8	123.78	7.36	54.29	-17.19	39.82	-6.26	171.51
2.6	-6.88	119.6	7.07	51.67	-16.84	37.52	-6.44	170.48
2.7	-6.95	115.98	6.8	48.92	-16.51	35.13	-6.63	169.32
2.8	-7.01	111.9	6.53	46.29	-16.18	32.68	-6.84	167.88
2.9	-7.05	108.47	6.27	43.48	-15.86	30.1	-7.07	166.08
3	-7.05	104.53	6.03	40.59	-15.57	27.48	-7.34	164.04
3.1	-7.04	101.44	5.79	37.57	-15.28	24.61	-7.62	161.54
3.2	-6.99	98.36	5.57	34.52	-15.02	21.76	-7.93	158.85
3.3	-6.97	96.27	5.27	30.79	-14.79	18.27	-8.39	155.19
3.4	-6.91	95.01	4.9	26.21	-14.61	13.73	-9.27	151.2
3.5	-6.57	96.52	3.93	20.85	-14.91	6.81	-11.77	153.29
3.6	-5.55	92.49	2.88	26.47	-16.53	12.14	-8.69	-178.82
3.7	-5.55	87.7	3.34	26.88	-15.16	15.77	-7.02	162.03
3.8	-5.53	85.33	3.41	24.19	-14.57	12.67	-7.15	152.24
3.9	-5.47	84.19	3.3	21.57	-14.26	10	-7.33	146.12
4	-5.31	82.62	3.12	18.7	-14.02	7.07	-7.47	140.74
4.1	-5.18	81.66	2.88	16.12	-13.89	4.33	-7.56	135.79
4.2	-5	80.5	2.65	13.67	-13.74	1.97	-7.62	131.3
4.3	-4.85	79.84	2.39	11.3	-13.61	-0.36	-7.65	126.93
4.4	-4.68	78.94	2.13	9.06	-13.51	-2.77	-7.66	122.93
4.5	-4.56	78.6	1.87	7.03	-13.43	-4.89	-7.67	119.12
4.6	-4.44	78.11	1.65	5.23	-13.35	-6.77	-7.7	115.86
4.7	-4.37	77.96	1.4	3.33	-13.27	-8.67	-7.73	112.46
4.8	-4.29	77.71	1.18	1.46	-13.17	-10.55	-7.81	109.32
4.9	-4.25	77.78	0.97	-0.29	-13.06	-12.37	-7.91	106.37
5	-4.21	77.6	0.77	-2.08	-12.95	-14.26	-8.06	103.68
5.1	-4.23	77.84	0.59	-3.78	-12.83	-16.05	-8.26	101.24
5.2	-4.22	77.68	0.42	-5.6	-12.71	-17.98	-8.5	99.01
5.3	-4.26	78	0.26	-7.35	-12.59	-19.83	-8.81	96.74
5.4	-4.3	78.17	0.11	-9.04	-12.48	-21.63	-9.15	95
5.5	-4.39	78.68	-0.03	-10.8	-12.35	-23.56	-9.64	93.12
5.6	-4.5	79.02	-0.17	-12.7	-12.21	-25.58	-10.28	91.58
5.7	-4.64	79.8	-0.3	-14.58	-12.07	-27.61	-11.05	90.16
5.8	-4.81	80.51	-0.42	-16.61	-11.94	-29.79	-12.05	89.15
5.9	-5.02	81.48	-0.53	-18.67	-11.81	-31.99	-13.32	88.95
6	-5.25	82.44	-0.66	-20.87	-11.68	-34.39	-14.85	89.83

Demo Board

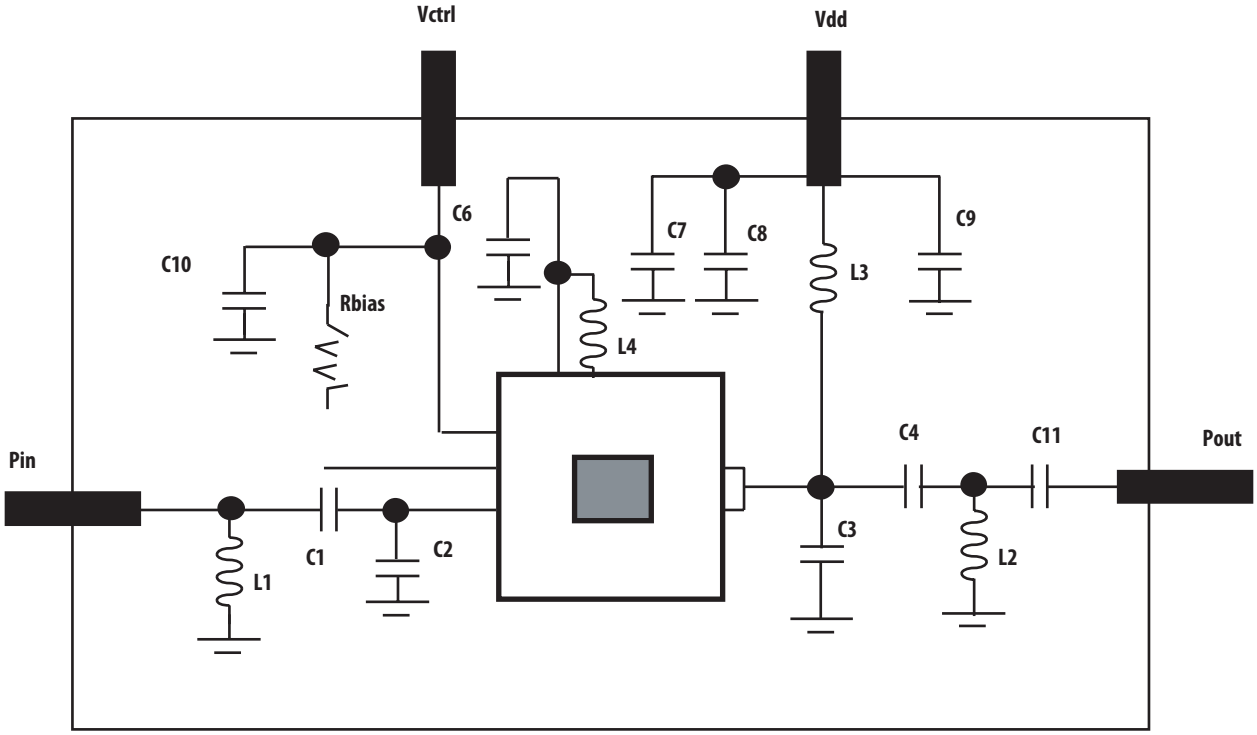


Figure 6. Demo board and application schematic

Demo Board Part List

Circuit Symbol	Size	Value	Part Number	Description
L1	0402	10nH	LLP1005-FH10NC (TOKO)	MLC Inductor
L2	0402	6.8nH	LLP1005-FH6N8C (TOKO)	MLC Inductor
L3	0402	8.2nH	LL1005-FHL8N2J (TOKO)	MLC Inductor
L4	0402	15nH	MLK1005S15NJ (TDK)	MLC Inductor
C1	0402	6pF	C1005C0G1H060D (TDK)	Ceramic Chip Capacitor
C2	0402	1.8pF	GRM1555C1H1R8CZ01B (Murata)	Ceramic Chip Capacitor
C3	0402	4.3pF	GRM1555C1H4R3CZ01B (Murata)	Ceramic Chip Capacitor
C4	0402	5.6pF	GRM1555C1H5R6CZ01B (Murata)	Ceramic Chip Capacitor
C6	0402	100pF	GRM1555C1H101JZ01B (Murata)	Ceramic Chip Capacitor
C7	0402	0.1uF	GRM155R71E103KA01B (Murata)	Ceramic Chip Capacitor
C8	0402	100pF	GRM1555C1H101JZ01B (Murata)	Ceramic Chip Capacitor
C9	0805	2.2uF	GRM21BR61E225KA12L (Murata)	Tantalum Capacitor
C10	0402	100pF	GRM1555C1H101JZ01B (Murata)	Ceramic Chip Capacitor
C11	0402	100pF	GRM1555C1H101JZ01B (Murata)	Ceramic Chip Capacitor

Note: Rbias is used to lower the quiescent current. Default is 0 ohm

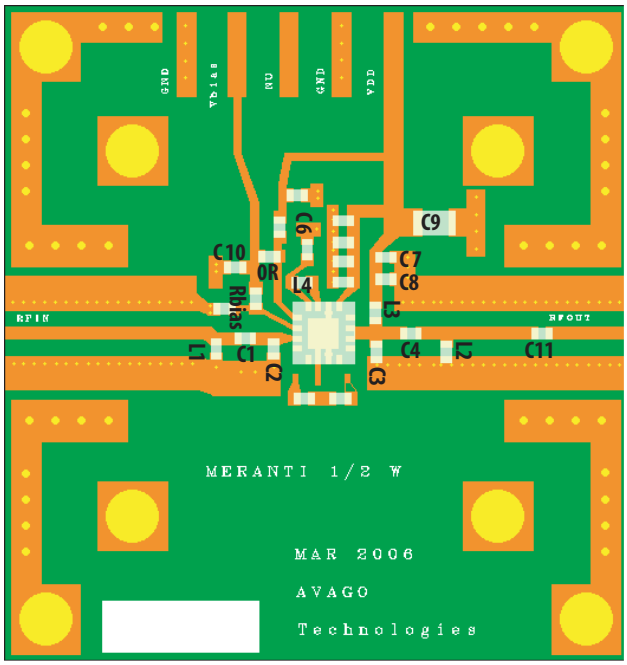


Figure 7. Demo board Layout

- Recommended PCB material is 10 mils Rogers RO4350, with FR4 backing for mechanical strength.
- Suggested component values may vary according to layout and PCB material.

MGA-30116 Typical Performance

T_A = +25°C, Vdd = 5V, Vctrl =5V, Input Signal=CW unless stated otherwise.

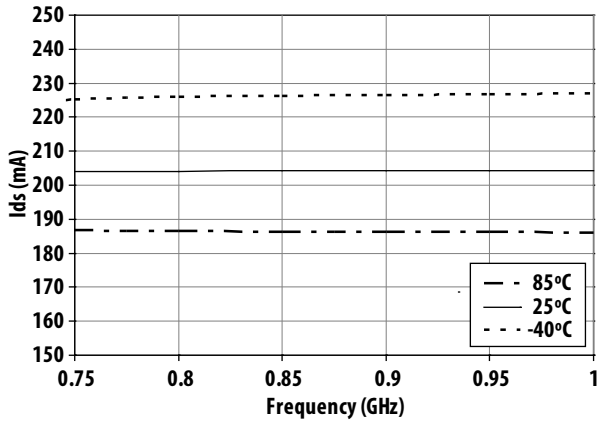


Figure 8. Over Temperature Ids vs Frequency

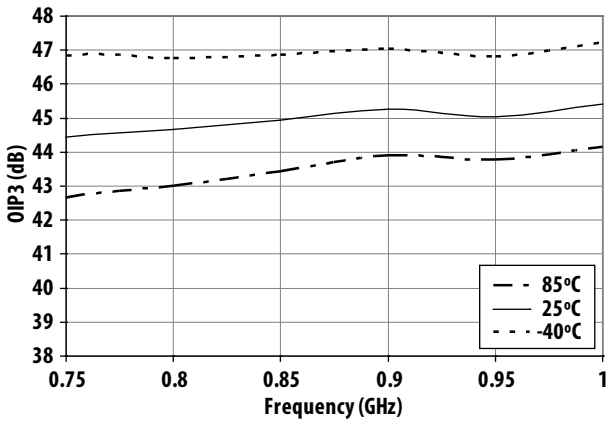


Figure 9. Over Temperature OIP3 vs Frequency

MGA-30116 Typical Performance

T_A = +25°C, Vdd = 5V, Vctrl =5V, Input Signal=CW unless stated otherwise.

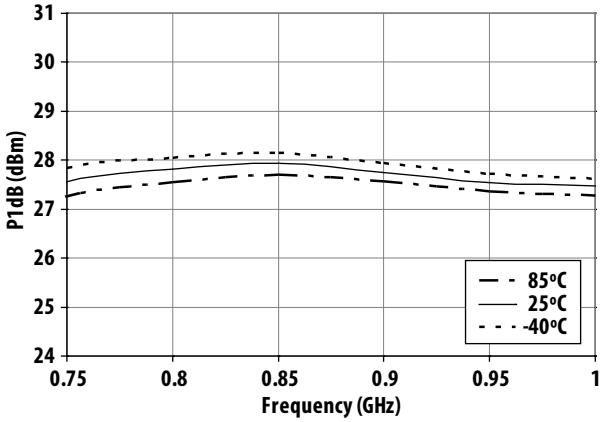


Figure 10. Over Temperature P1dB vs Frequency

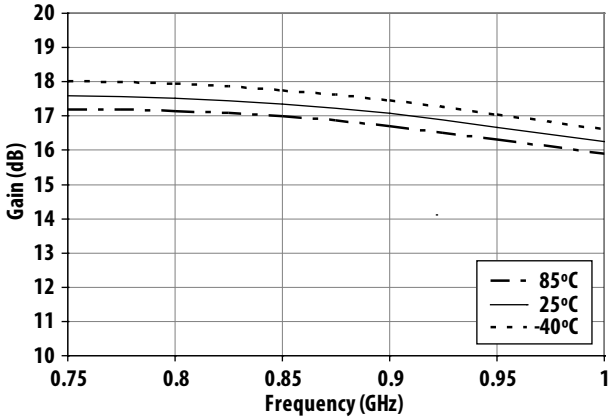


Figure 11. Over Temperature Gain vs Frequency

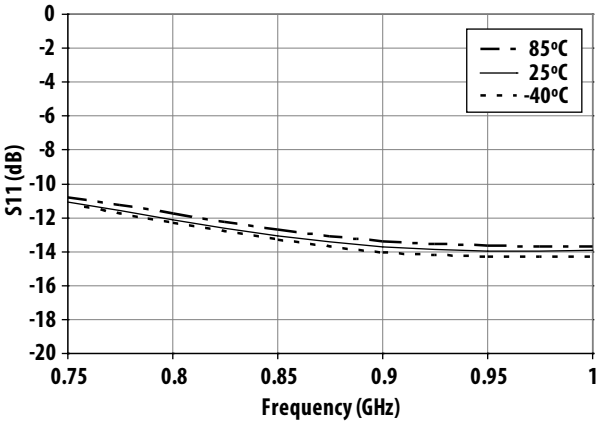


Figure 12. Over Temperature S11 vs Frequency

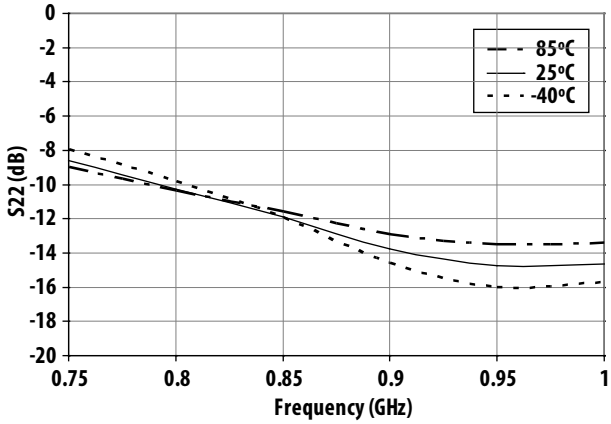


Figure 13. Over Temperature S22 vs Frequency

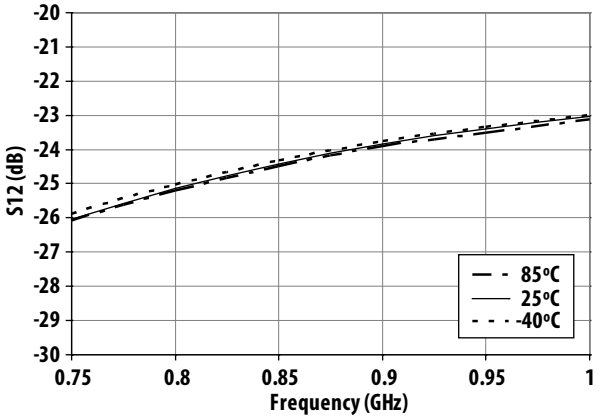


Figure 14. Over Temperature S12 vs Frequency

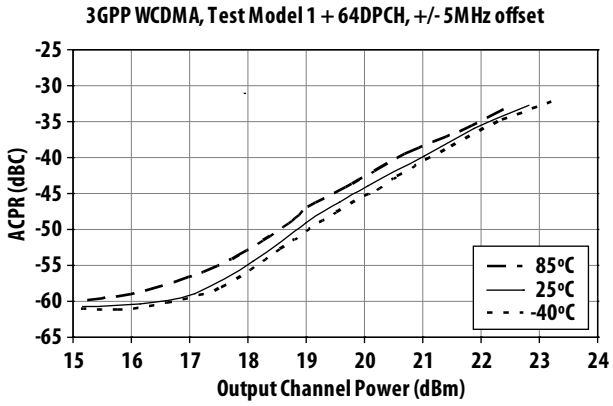
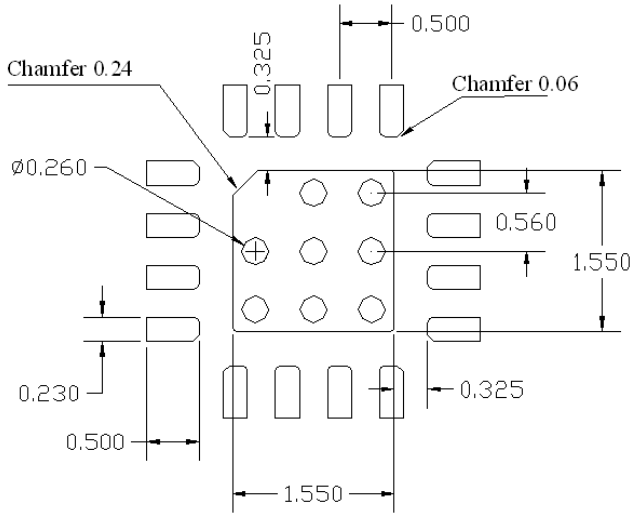
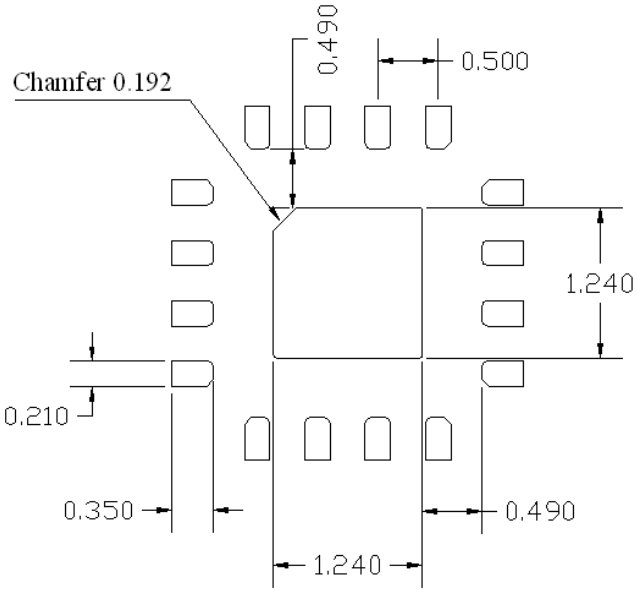


Figure 15. Over Temperature ACPR (900MHz) Vs Pout

PCB Layout and Stencil Design

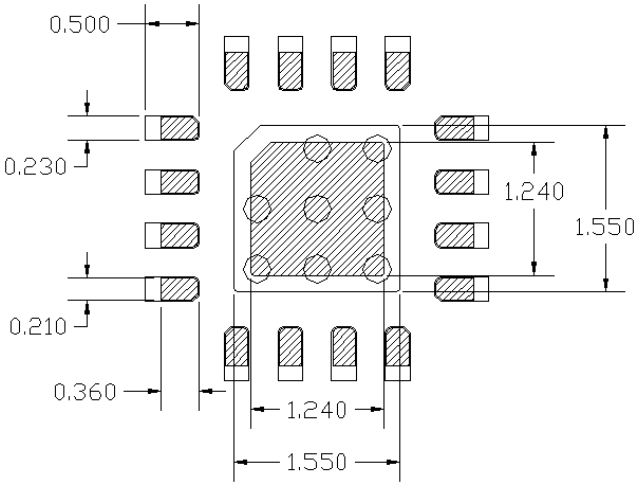


PCB Land Pattern (Top View)



Stencil Outline

Notes:
1. All dimensions are in milimeters.

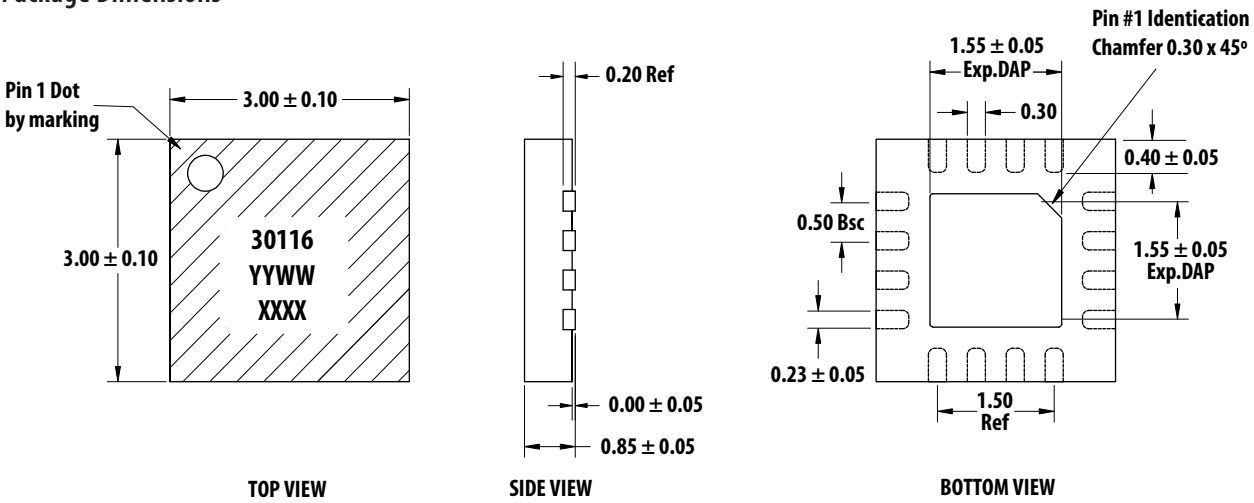


Combined PCB and stencil layout

Part Number Ordering Information

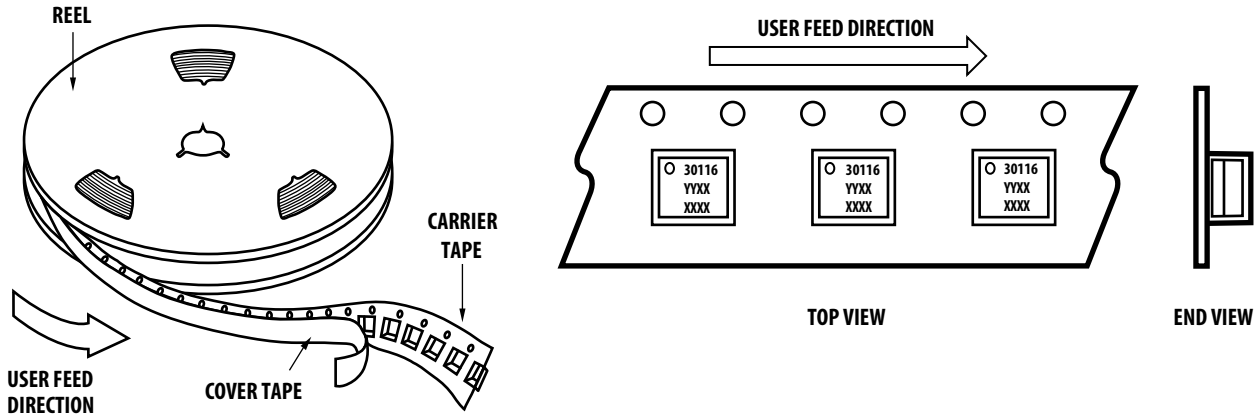
Part Number	No. of Devices	Container
MGA-30116-TR1G	1000	7″ Reel
MGA-30116-TR2G	3000	13″ Reel
MGA-30116-BLKG	100	antistatic bag

Package Dimensions

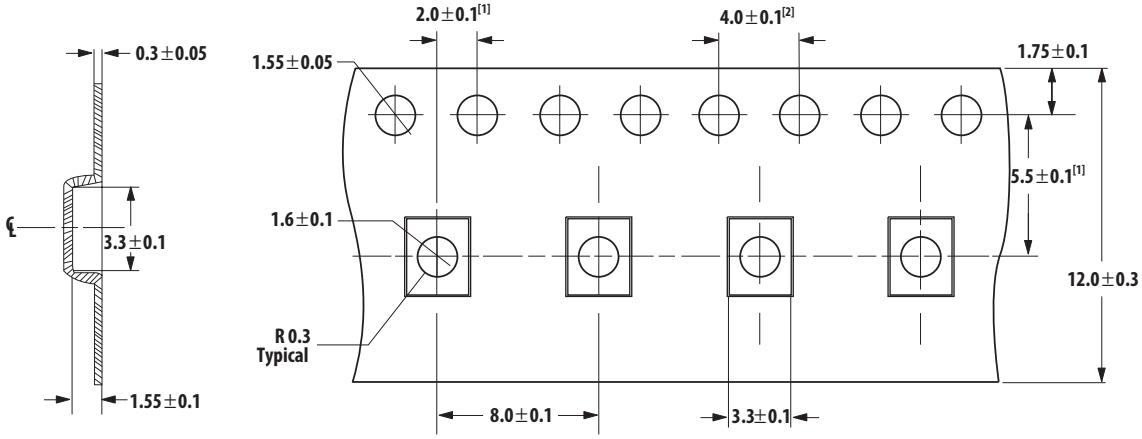


Notes:
1. All dimensions are in milimeters
2. Dimensions are inclusive of plating
3. Dimensions are exclusive of mold flash and metal burr

Device Orientation

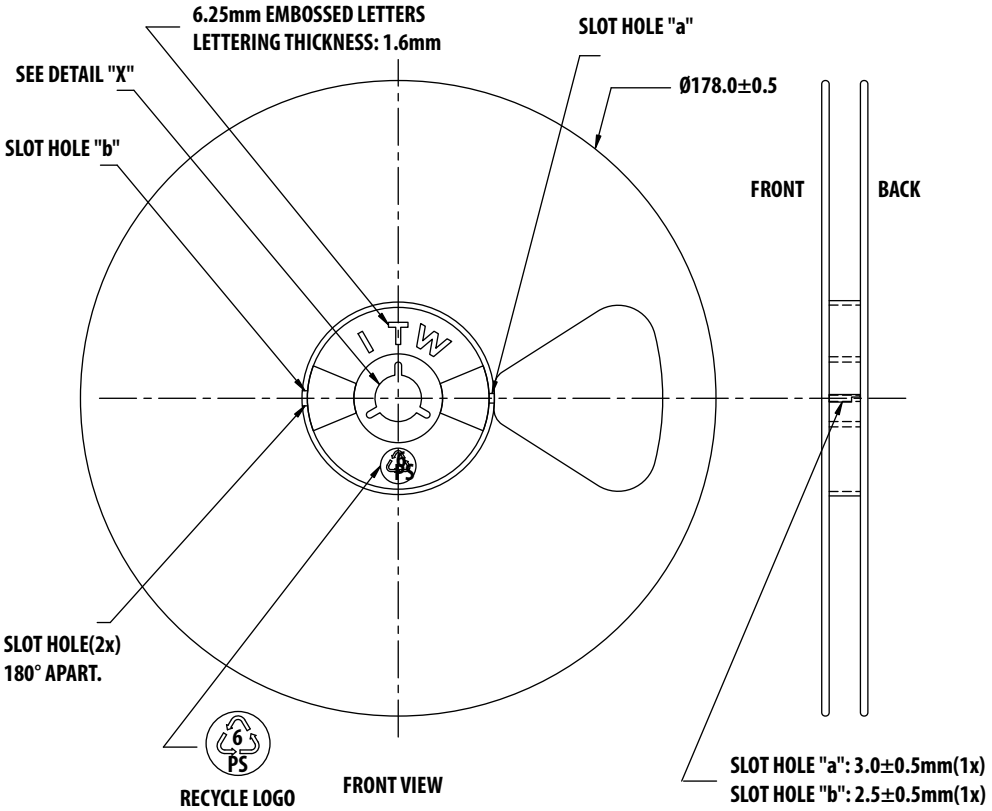


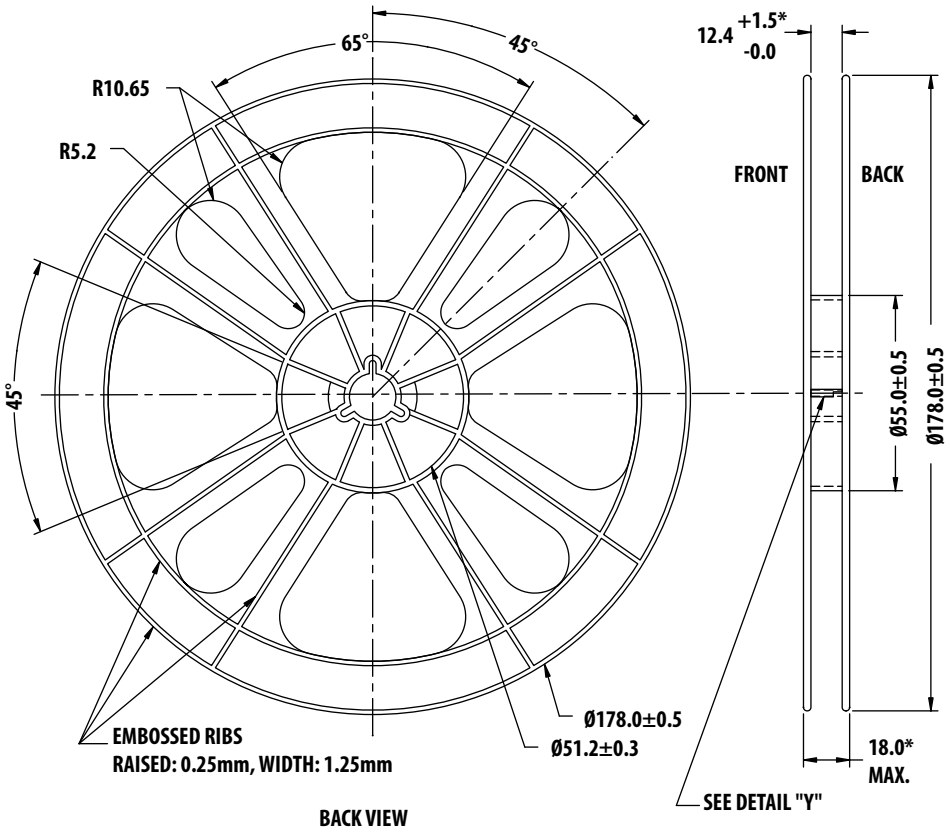
Tape Dimensions

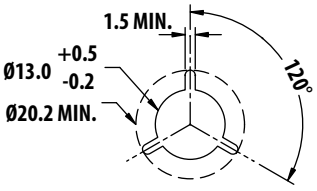


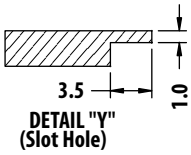
Notes:
1. Measured from centerline of sprocket hole to centerline of pocket
2. Cumulative tolerance of 10 sprocket holes is ± 0.20
3. All dimensions in millimeter unless otherwise stated

Reel Dimensions - 7 inch

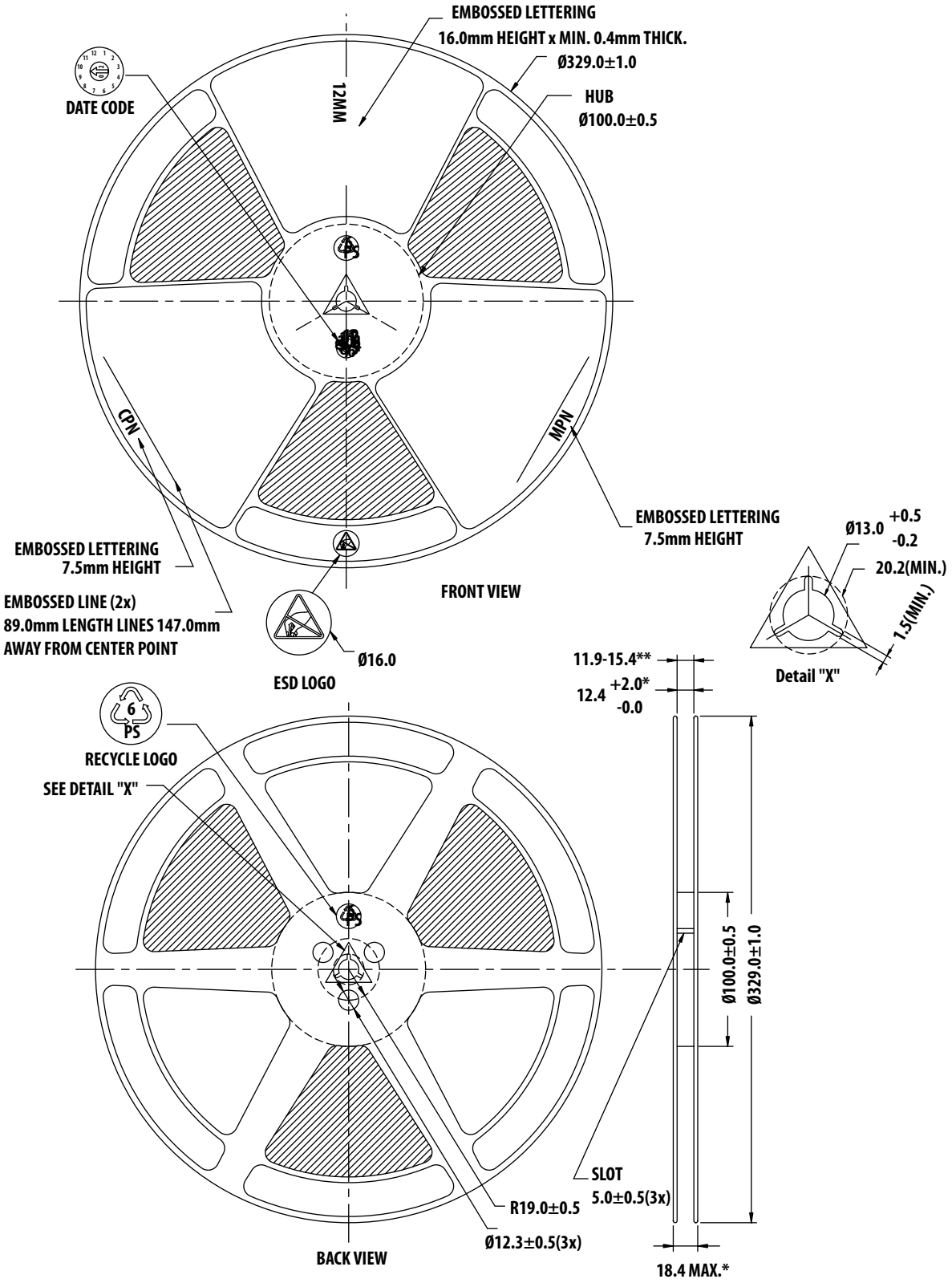








Reel Dimensions - 13 inch



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