BLF25M612; BLF25M612G

Power LDMOS transistor

Rev. 3 — 16 December 2014 Product data sheet

1. Product profile

1.1 General description

12 W LDMOS power transistor for Industrial, Scientific and Medical (ISM) applications at frequencies from 2400 MHz to 2500 MHz.

The BLF25M612 and BLF25M612G are drivers designed for high power CW applications and is assembled in a high performance ceramic package.

Table 1. Typical performance

RF performance at T_{case} = 25 °C in a common source class-AB production test circuit.

Test signal	f	V_{DS}	$P_{L(AV)}$	G_p	η_D
	(MHz)	(V)	(W)	(dB)	(%)
CW	2450	28	12	19	60

1.2 Features and benefits

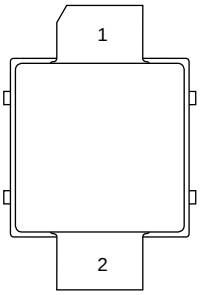
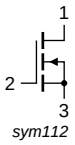
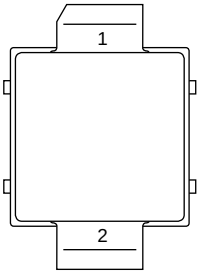
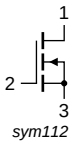
- High efficiency
- High power gain
- Excellent ruggedness
- Excellent thermal stability
- Integrated ESD protection
- Designed for broadband operation (2400 MHz to 2500 MHz)
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- Industrial, scientific and medical applications in the frequency range 2400 MHz to 2500 MHz (this product is qualified according to the solid state cooking profile)

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
BLF25M612 (SOT975B)			
1	drain		
2	gate		
3	source [1]		
BLF25M612G (SOT975C)			
1	drain		
2	gate		
3	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF25M612	-	earless flanged ceramic package; 2 leads	SOT975B
BLF25M612G	-	earless flanged ceramic package; 2 leads	SOT975C

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		–0.5	+13	V
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature	[1]	-	225	°C

[1] Continuous use at maximum temperature will affect reliability.

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5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-case)}$	thermal resistance from junction to case	T_{case} = 80 °C; P_L = 12 W	4.0	K/W

6. Characteristics

Table 6. DC characteristics

T_j = 25 °C per section; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.18 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 18 mA	1.4	1.9	2.4	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 28 V	-	-	1.4	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	-	3.2	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	140	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 0.9 A	-	1.3	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 0.6 A	-	0.8	1.3	Ω

Table 7. RF characteristics

Test signal: CW at f = 2450 MHz; RF performance at V_{DS} = 28 V; I_{Dq} = 10 mA; T_{case} = 25 °C; unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	P_L = 12 W	17	19	-	dB
RL_{in}	input return loss	P_L = 12 W	-	–14	–10	dB
η_D	drain efficiency	P_L = 12 W	54	60	-	%

7. Test information

7.1 Ruggedness in class-AB operation

The BLF25M612 and BLF25M612G are capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 28 V; I_{Dq} = 10 mA; P_L = 12 W (CW); f = 2450 MHz.

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7.2 Impedance information

Table 8. Typical impedance

Measured load-pull data. Typical values unless otherwise specified.

f	Z_S	Z_L
(MHz)	(Ω)	(Ω)
2400	3.0 – 11.4j	4.17 – 3.3j
2450	3.7 – 11.4j	4.3 – 2.7j
2500	3.8 – 11.4j	4.7 – 4.6j

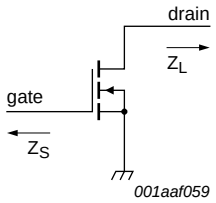
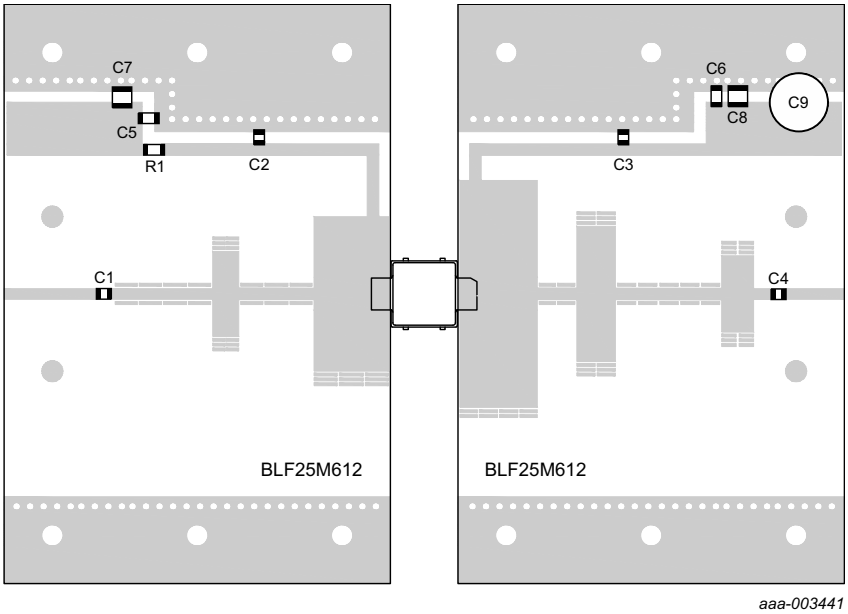


Fig 1. Definition of transistor impedance

7.3 Test circuit



Printed-Circuit Board (PCB): Rogers 4350B; ε_r = 3.5; thickness = 0.508 mm; thickness copper plating = 35 μm

See Table 9 for a list of components.

Fig 2. Component layout

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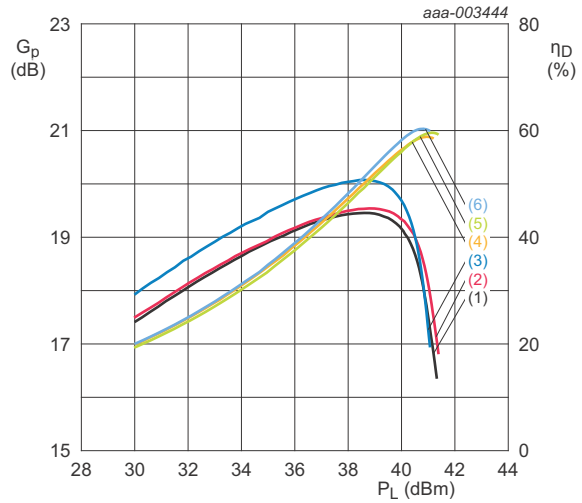
Table 9. List of components

For test circuit see Figure 2.

Component	Description	Value	Remarks
C1, C2, C3, C4	multilayer ceramic chip capacitor	15 pF	ATC100A
C5, C6	multilayer ceramic chip capacitor	220 nF	SMD 1206
C7, C8	multilayer ceramic chip capacitor	4.7 μF, 50 V	
C9	electrolytic capacitor	100 μF, 63 V	
R1	SMD resistor	7.5 Ω	SMD 0805

7.4 Graphical data



V_{DS} = 28 V; I_{Dq} = 10 mA.

(1) G_p at f = 2400 MHz

(2) G_p at f = 2450 MHz

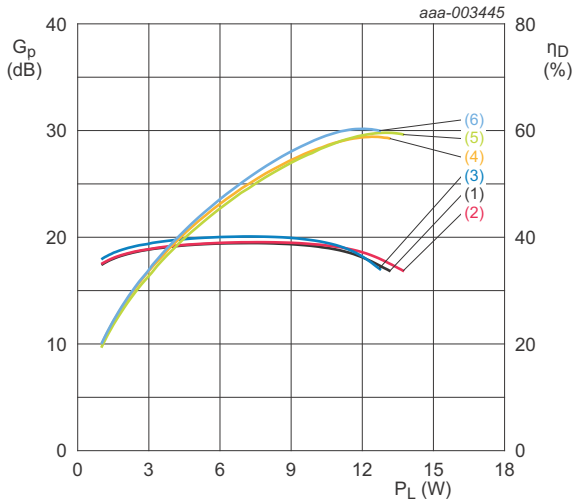
(3) G_p at f = 2500 MHz

(4) η_D at f = 2400 MHz

(5) η_D at f = 2450 MHz

(6) η_D at f = 2500 MHz

Fig 3. Power gain and drain efficiency as function of load power; typical values



V_{DS} = 28 V; I_{Dq} = 10 mA.

(1) G_p at f = 2400 MHz

(2) G_p at f = 2450 MHz

(3) G_p at f = 2500 MHz

(4) η_D at f = 2400 MHz

(5) η_D at f = 2450 MHz

(6) η_D at f = 2500 MHz

Fig 4. Power gain and drain efficiency as function of load power; typical values

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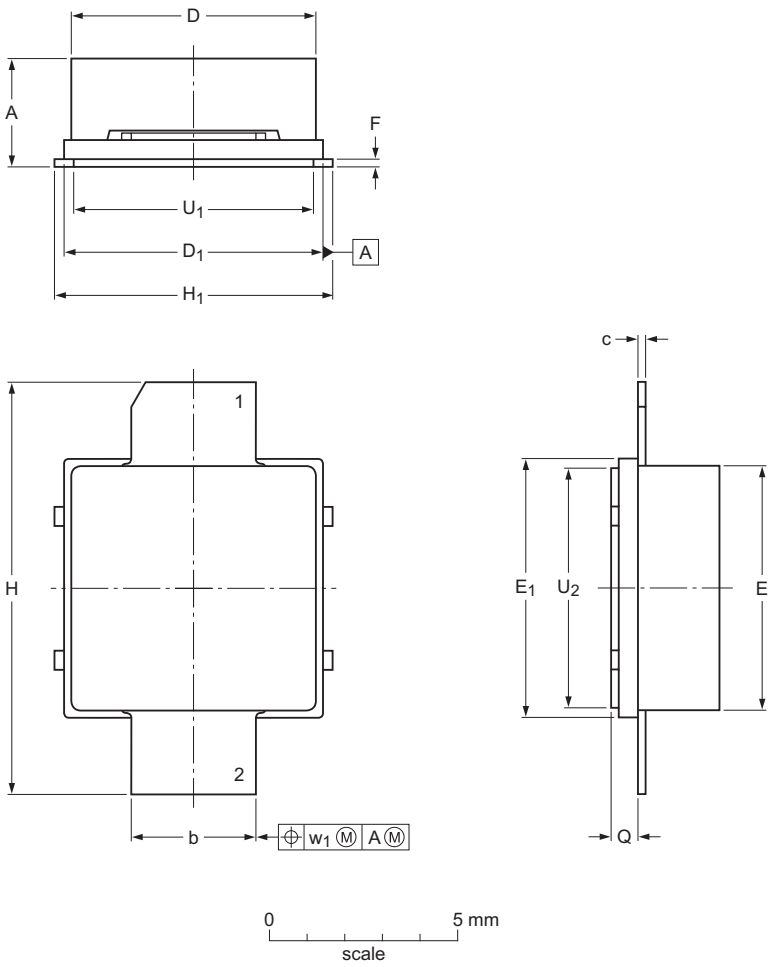
8. Package outline

Earless flanged ceramic package; 2 leads **SOT975B**



Dimensions (mm dimensions are derived from the original inch dimensions)

Unit		A	b	c	D	D_1	E	E_1	F	H	H_1	Q	U_1	U_2	w_1
mm	max	3.15	3.38	0.23	6.55	6.93	6.55	6.93	0.23	11.05	7.49	0.76	6.43	6.43	0.51
	nom														
	min	2.59	3.23	0.18	6.40	6.78	6.40	6.78	0.18	10.80	6.73	0.66	6.27	6.27	
inches	max	0.124	0.133	0.009	0.258	0.273	0.258	0.273	0.009	0.435	0.295	0.030	0.253	0.253	0.02
	nom														
	min	0.102	0.127	0.007	0.252	0.267	0.252	0.267	0.007	0.425	0.265	0.026	0.247	0.247	

sot975b_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT975B						~~07-09-28~~ 14-10-20

Fig 5. Package outline SOT975B

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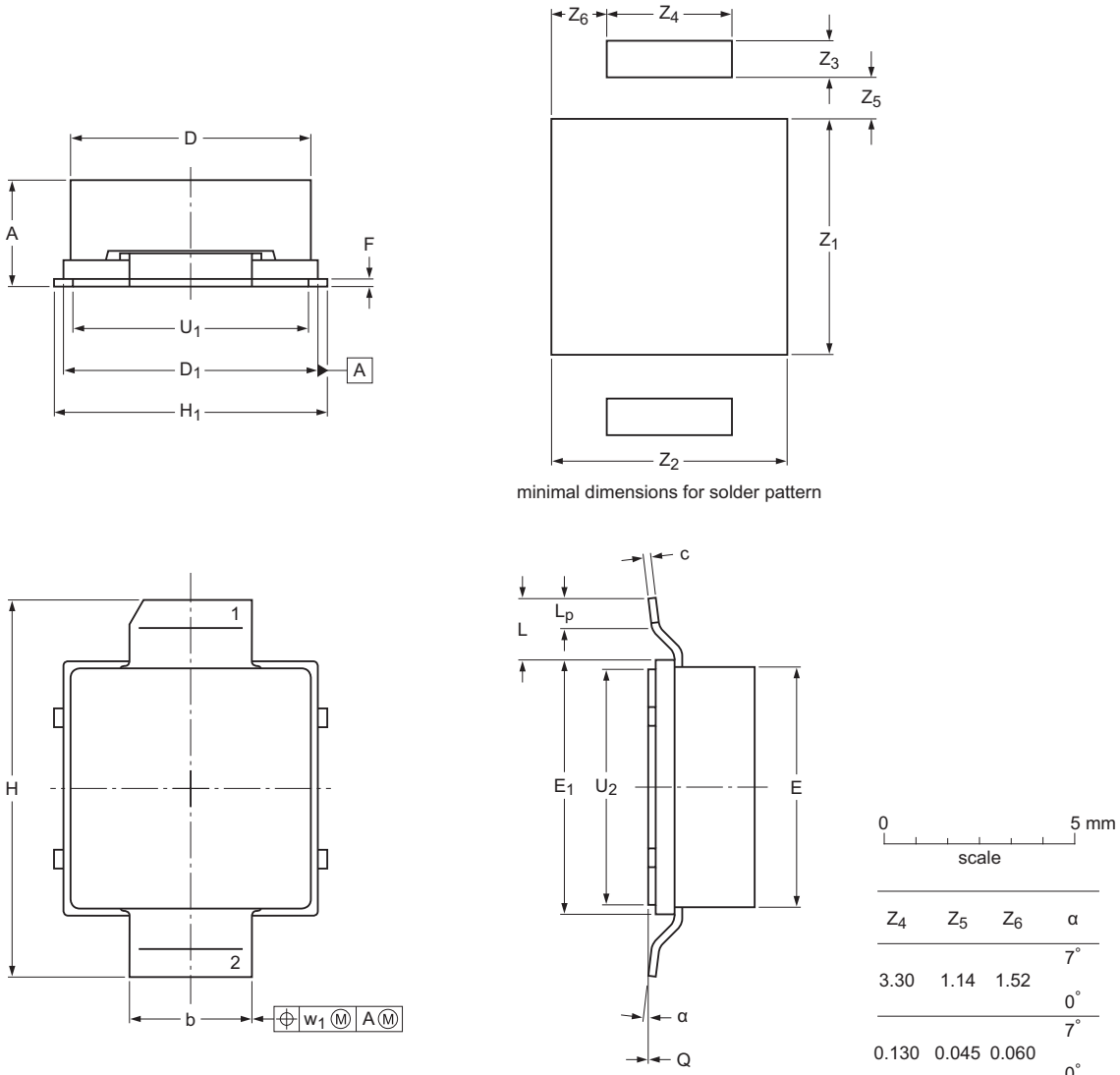
Earless flanged ceramic package; 2 leads **SOT975C**



Z4	Z5	Z6	α
3.30	1.14	1.52	7° / 0°
0.130	0.045	0.060	7° / 0°

Dimensions (mm dimensions are derived from the original inch dimensions)

Unit		A	b	c	D	D_1	E	E_1	F	H	H_1	L	L_p	Q	U_1	U_2	w_1	Z_1	Z_2	Z_3
mm	max	3.15	3.38	0.23	6.55	6.93	6.55	6.93	0.23	10.29	7.49		1.02	+0.05	6.43	6.43				
	nom											1.65					0.51	6.35	6.35	1.02
	min	2.59	3.23	0.18	6.40	6.78	6.40	6.78	0.18	10.03	6.73		0.51	-0.05	6.27	6.27				
inches	max	0.124	0.133	0.009	0.258	0.273	0.258	0.273	0.009	0.405	0.295		0.040	+0.002	0.253	0.253				
	nom											0.065					0.020	0.250	0.250	0.040
	min	0.102	0.127	0.007	0.252	0.267	0.252	0.267	0.007	0.395	0.265		0.020	-0.002	0.247	0.247				

sot975c_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT975C						~~08-07-10~~ 14-10-13

Fig 6. Package outline SOT975C

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9. Handling information

CAUTION	
	This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices. Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

10. Abbreviations

Table 10. Abbreviations

Acronym	Description
CW	Continuous Wave
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
SMD	Surface Mounted Device
VSWR	Voltage Standing-Wave Ratio

11. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF25M612_BLF25M612G v.3	20141216	Product data sheet	-	BLF25M612_BLF25M612G v.2
Modifications	• Package outline drawings updated.			
BLF25M612_BLF25M612G v.2	20130620	Product data sheet	-	BLF25M612G v.1
BLF25M612G v.1	20120605	Objective data sheet	-	-

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Document status[1][2]	Product status[3]	Definition
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