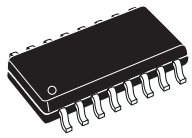
L6566BH

Multimode controller for SMPS

Datasheet — production data

Features

- Selectable multimode operation: fixed frequency or quasi-resonant
- On-board 840 V high voltage startup
- Advanced light load management
- Low quiescent current (< 3 mA)
- Adaptive UVLO
- Line feedforward for constant power capability vs. mains voltage
- Pulse-by-pulse OCP, shutdown on overload (latched or auto-restart)
- Transformer saturation detection
- Programmable frequency modulation for EMI reduction
- Latched or auto-restart OVP
- Brownout protection



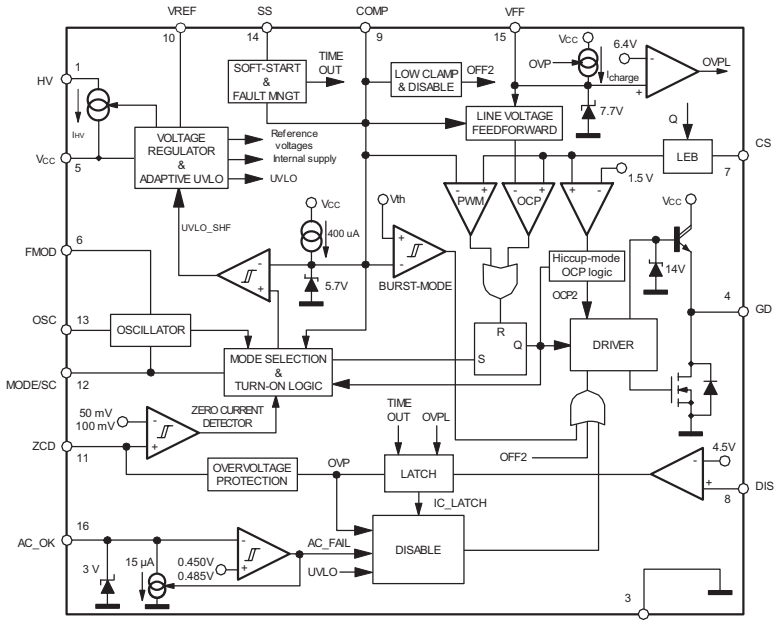
SO16N

- -600/+800 mA totem pole gate driver with active pull-down during UVLO
- SO16N package

Applications

- Industrial SMPS
- SMPS running off rectified 3-phase input line

Figure 1. Block diagram



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Contents

1 Description 6

2 Pin settings 8

2.1 Connections 8

2.2 Pin description 8

3 Electrical data 11

3.1 Maximum rating 11

3.2 Thermal data 11

4 Electrical characteristics 12

5 Application information 16

5.1 High voltage startup generator 17

5.2 Zero-current detection and triggering block; oscillator block 19

5.3 Burst-mode operation at no load or very light load 22

5.4 Adaptive UVLO 23

5.5 PWM control block 24

5.6 PWM comparator, PWM latch and voltage feedforward blocks 25

5.7 Hiccup-mode OCP 28

5.8 Frequency modulation 29

5.9 Latched disable function 31

5.10 Soft-start and delayed latched shutdown upon overcurrent 32

5.11 OVP block 33

5.12 Brownout protection 36

5.13 Slope compensation 39

5.14 Summary of L6566BH power management functions 39

6 Application examples and ideas 43

7 Package mechanical data 46

8 Order codes 49

9 Revision history 50

List of tables

Table 1. Pin functions 8
Table 2. Absolute maximum ratings 11
Table 3. Thermal data. 11
Table 4. Electrical characteristics 12
Table 5. L6566BH light load management features 40
Table 6. L6566BH protection 40
Table 7. External circuits that determine IC behavior upon OVP and OCP 44
Table 8. SO16N mechanical data. 46
Table 9. Order codes 49
Table 10. Document revision history 50

List of figures

Figure 1. Block diagram . . . 1
Figure 2. Typical system block diagram . . . 7
Figure 3. Pin connection (through top view) . . . 8
Figure 4. Multimode operation with QR option active . . . 16
Figure 5. High voltage startup generator: internal schematic . . . 17
Figure 6. Timing diagram: normal power-up and power-down sequences . . . 18
Figure 7. Timing diagram showing short-circuit behavior (SS pin clamped at 5 V) . . . 19
Figure 8. V_{HV} rating vs. temperature . . . 19
Figure 9. Drain ringing cycle skipping as the load is gradually reduced . . . 20
Figure 10. Operation of ZCD, triggering and oscillator blocks (QR option active) . . . 22
Figure 11. Load-dependent operating modes: timing diagrams . . . 23
Figure 12. Addition of an offset to the current sense lowers the burst-mode operation threshold . . . 23
Figure 13. Adaptive UVLO block . . . 24
Figure 14. Possible feedback configurations that can be used with the L6566BH . . . 24
Figure 15. Externally controlled burst-mode operation by driving the COMP pin: timing diagram . . . 25
Figure 16. Typical power capability change vs. input voltage in QR flyback converters . . . 26
Figure 17. Left: overcurrent setpoint vs. VFF voltage; right: line feedforward function block . . . 27
Figure 18. Hiccup-mode OCP: timing diagram . . . 29
Figure 19. Frequency modulation circuit . . . 30
Figure 20. Operation after latched disable activation: timing diagram . . . 32
Figure 21. Soft-start pin operation under different operating conditions and settings . . . 33
Figure 22. OVP function: internal block diagram . . . 34
Figure 23. OVP function: timing diagram . . . 35
Figure 24. Maximum allowed duty cycle vs. switching frequency for correct OVP detection . . . 36
Figure 25. Brownout protection: internal block diagram and timing diagram . . . 37
Figure 26. Voltage sensing techniques to implement brownout protection with the L6566BH . . . 38
Figure 27. Slope compensation waveforms . . . 39
Figure 28. Typical low-cost application schematic . . . 43
Figure 29. Typical full-feature application schematic (QR operation) . . . 43
Figure 30. Typical full-feature application schematic (FF operation) . . . 44
Figure 31. Frequency foldback at light load (FF operation) . . . 45
Figure 32. Latched shutdown upon mains overvoltage . . . 45
Figure 33. SO16N package drawing . . . 47
Figure 34. Recommended footprint (dimensions are in mm) . . . 48

1 Description

The L6566BH is an extremely versatile current-mode primary controller IC, specifically designed for high-performance offline flyback converters running off rectified 3-phase input lines. It is also suited to single-stage, single-switch, input-current-shaping converters (single-stage PFC) for applications that must comply with EN61000-3-2 or JEITA-MITI regulations.

Both fixed-frequency (FF) and quasi-resonant (QR) operation are supported. The user can choose either of the two depending on application needs. The device features an externally programmable oscillator: it defines the converter switching frequency in FF mode and the maximum allowed switching frequency in QR mode.

When FF operation is selected, the ICs work as a standard current-mode controller with a maximum duty cycle limited to 70% min. The oscillator frequency can be modulated to mitigate EMI emissions.

QR operation, when selected, occurs at heavy load and is achieved through a transformer demagnetization sensing input that triggers MOSFET turn-on. Under some conditions, ZVS (zero-voltage switching) can be achieved. The converter's power capability rise with the mains voltage is compensated by line voltage feedforward. At medium and light load, as the QR operating frequency equals the oscillator frequency, a function (valley skipping) is activated to prevent further frequency rise and keep the operation as close to ZVS as possible.

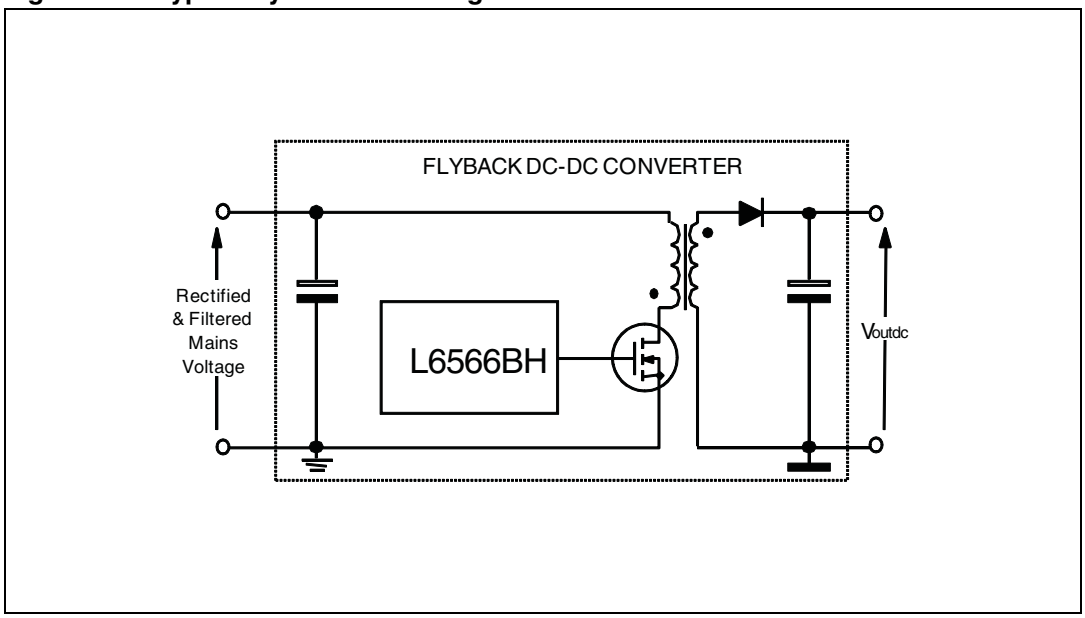
With either FF or QR operation, at very light load the ICs enter a controlled burst-mode operation that, along with the built-in, non-dissipative, high-voltage startup circuit and the low quiescent current, helps keep the consumption from the mains low and meet energy saving recommendations.

An innovative adaptive UVLO helps minimize the issues related to the fluctuations of the self-supply voltage due to transformer parasites.

The protection functions included in this device are: not-latched input undervoltage (brownout), output OVP (auto-restart or latch-mode selectable), a first-level OCP with delayed shutdown to protect the system during overload or short-circuit conditions (auto-restart or latch-mode selectable), and a second-level OCP that is invoked when the transformer saturates or there is a short-circuit of the secondary diode. A latched disable input allows easy implementation of OTP with an external NTC, while an internal shutdown prevents IC overheating.

Programmable soft-start, leading-edge blanking on the current sense input for greater noise immunity, slope compensation (in FF mode only), and a shutdown function for externally controlled burst-mode operation or remote ON/OFF control complete the features of this device.

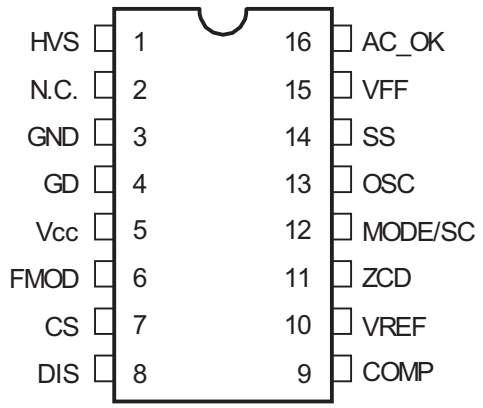
Figure 2. Typical system block diagram



2 Pin settings

2.1 Connections

Figure 3. Pin connection (through top view)



2.2 Pin description

Table 1. Pin functions

N°	Pin	Function
1	HVS	High voltage startup. The pin, able to withstand 840 V, is to be tied directly to the rectified mains voltage. A 1 mA internal current source charges the capacitor connected between the Vcc pin (5) and GND pin (3) until the voltage on the Vcc pin reaches the turn-on threshold, it is then shut down. Normally, the generator is re-enabled when the Vcc voltage falls below 5 V to ensure a low power throughput during short-circuit. Otherwise, when a latched protection is tripped the generator is re-enabled 0.5 V below the turn-on threshold, to keep the latch supplied; or, when the IC is turned off by the COMP pin (9) pulled low, the generator is active just below the UVLO threshold to allow a faster restart.
2	N.C.	Not internally connected. Provision for clearance on the PCB to meet safety requirements.
3	GND	Ground. Current return for both the signal part of the IC and the gate drive. All of the ground connections of the bias components should be tied to a track going to this pin and kept separate from any pulsed current return.
4	GD	Gate driver output. The totem pole output stage is able to drive Power MOSFETs and IGBTs with a peak current capability of 800 mA source/sink.

Table 1. Pin functions (continued)

N°	Pin	Function
5	Vcc	Supply voltage of both the signal part of the IC and the gate driver. The internal high voltage generator charges an electrolytic capacitor connected between this pin and GND (pin 3) as long as the voltage on the pin is below the turn-on threshold of the IC, after that it is disabled and the chip is turned on. The IC is disabled as the voltage on the pin falls below the UVLO threshold. This threshold is reduced at light load to counteract the natural reduction of the self-supply voltage. Sometimes a small bypass capacitor (0.1 µF typ.) to GND might be useful to obtain a clean bias voltage for the signal part of the IC.
6	FMOD	Frequency modulation input. When FF mode operation is selected, a capacitor connected from this pin to GND (pin 3) is alternately charged and discharged by internal current sources. As a result, the voltage on the pin is a symmetrical triangular waveform with the frequency related to the capacitance value. By connecting a resistor from this pin to pin 13 (OSC) it is possible to modulate the current sourced by the OSC pin and then the oscillator frequency. This modulation is to reduce the peak value of EMI emissions by means of a spread-spectrum action. If the function is not used, the pin is left open.
7	CS	Input to the PWM comparator. The current flowing in the MOSFET is sensed through a resistor, the resulting voltage is applied to this pin and compared with an internal reference to determine MOSFET turn-off. The pin is equipped with 150 ns min. blanking time after the gate-drive output goes high for improved noise immunity. A second comparison level located at 1.5 V latches the device OFF and reduces its consumption in the case of transformer saturation or secondary diode short-circuit. The information is latched until the voltage on the Vcc pin (5) goes below the UVLO threshold, therefore resulting in intermittent operation. A logic circuit improves sensitivity to temporary disturbances.
8	DIS	IC latched disable input. Internally, the pin connects a comparator that, when the voltage on the pin exceeds 4.5 V, latches OFF the IC and brings its consumption to a lower value. The latch is cleared as the voltage on the Vcc pin (5) goes below the UVLO threshold, but the HV generator keeps the Vcc voltage high (see pin 1 description). It is then necessary to recycle the input power to restart the IC. For a quick restart, pull pin 16 (AC_OK) below the disable threshold (see pin 16 description). Bypass the pin with a capacitor to GND (pin 3) to reduce noise pick-up. Ground the pin if the function is not used.
9	COMP	Control input for loop regulation. The pin is driven by the phototransistor (emitter-grounded) of an optocoupler to modulate its voltage by modulating the current sunk. A capacitor placed between the pin and GND (3), as close to the IC as possible to reduce noise pick-up, sets a pole in the output-to-control transfer function. The dynamics of the pin are in the 2.5 to 5 V range. A voltage below an internally defined threshold activates burst-mode operation. The voltage at the pin is bottom-clamped at about 2 V. If the clamp is externally overridden and the voltage is pulled below 1.4 V, the IC shuts down.
10	VREF	An internal generator furnishes an accurate voltage reference (5 V ± 2%) that can be used to supply few mA to an external circuit. A small film capacitor (0.1 µF typ.), connected between this pin and GND (3), is recommended to ensure the stability of the generator and to prevent noise from affecting the reference. This reference is internally monitored by a separate auxiliary reference and any failure or drift causes the IC to latch OFF.

Table 1. Pin functions (continued)

N°	Pin	Function
11	ZCD	Transformer demagnetization sensing input for quasi-resonant operation and OVP input. The pin is externally connected to the transformer's auxiliary winding through a resistor divider. A negative-going edge triggers MOSFET turn-on if QR mode is selected. A voltage exceeding 5 V shuts the IC down and brings its consumption to a lower value (OVP). Latch OFF or auto-restart mode is selectable externally. This function is strobed and digitally filtered to increase noise immunity.
12	MODE/SC	Operating mode selection. If the pin is connected to the VREF pin (7), quasi-resonant operation is selected, the oscillator (pin 13, OSC) determines the maximum allowed operating frequency. Fixed-frequency operation is selected if the pin is not tied to VREF, in which case the oscillator determines the actual operating frequency, the maximum allowed duty cycle is set at 70% min. and the pin delivers a voltage ramp synchronized to the oscillator when the gate-drive output is high; the voltage delivered is zero while the gate-drive output is low. The pin is to be connected to pin CS (7) via a resistor for slope compensation.
13	OSC	Oscillator pin. The pin is an accurate 1 V voltage source, and a resistor connected from the pin to GND (pin 3) defines a current. This current is internally used to set the oscillator frequency that defines the maximum allowed switching frequency of the L6566BH, if working in QR mode, or the operating switching frequency if working in FF mode.
14	SS	Soft-start current source. At startup, a capacitor Css between this pin and GND (pin 3) is charged with an internal current generator. During the ramp, the internal reference clamp on the current sense pin (7, CS) rises linearly starting from zero to its final value, therefore causing the duty cycle to increase progressively starting from zero as well. During soft-start the adaptive UVLO function and all functions monitoring the COMP pin are disabled. The soft-start capacitor is discharged whenever the supply voltage of the IC falls below the UVLO threshold. The same capacitor is used to delay IC shutdown (latch OFF or auto-restart mode selectable) after detecting an overload condition (OLP).
15	VFF	Line voltage feedforward input. The information on the converter's input voltage is fed into the pin through a resistor divider and is used to change the setpoint of the pulse-by-pulse current limitation (the higher the voltage, the lower the setpoint). The linear dynamics of the pin ranges from 0 to 3 V. A voltage higher than 3 V makes the IC stop switching. If feedforward is not desired, tie the pin to GND (pin 3) directly if a latch-mode OVP is not required (see pin 11, ZCD) or through a 10 kΩ min. resistor if a latch-mode OVP is required. Bypass the pin with a capacitor to GND (pin 3) to reduce noise pick-up.
16	AC_OK	Brownout protection input. A voltage below 0.45 V shuts down (not latched) the IC, lowers its consumption and clears the latch set by latched protection (DIS > 4.5 V, SS > 6.4 V, VFF > 6.4 V). IC operation is re-enabled as the voltage exceeds 0.45 V. The comparator is provided with current hysteresis: an internal 15 µA current generator is ON as long as the voltage on the pin is below 0.45 V and is OFF if this value is exceeded. Bypass the pin with a capacitor to GND (pin 3) to reduce noise pick-up. Tie to Vcc with a 220 to 680 kW resistor if the function is not used.

3 Electrical data

3.1 Maximum rating

Table 2. Absolute maximum ratings

Symbol	Pin	Parameter	Value	Unit
V_{HVS}	1	Voltage range (referred to ground) @ 25 °C	-0.3 to 840	V
I_{HVS}	1	Output current	Self-limited	
V_{CC}	5	IC supply voltage (Icc = 20 mA)	Self-limited	
V_{FMOD}	6	Voltage range	-0.3 to 2	V
V_{max}	7, 8, 10, 14	Analog inputs and outputs	-0.3 to 7	V
V_{max}	9, 15, 16	Maximum pin voltage (Ipin ≤1 mA)	Self-limited	
I_{ZCD}	11	Zero-current detector max. current	±5	mA
$V_{MODE/SC}$	12	Voltage range	-0.3 to 5.3	V
V_{OSC}	13	Voltage range	-0.3 to 3.3	V
P_{TOT}		Power dissipation @ T_A = 50 °C	0.75	W
T_{STG}		Storage temperature	-55 to 150	°C
T_J		Junction operating temperature range	-40 to 150	°C

3.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction to ambient	120	°C/W

4 Electrical characteristics

(T_J = -25 to 125 °C, V_{CC} = 12, C_O = 1 nF; MODE/SC = V_{REF}, R_T = 20 kΩ from OSC to GND, unless otherwise specified.)

Table 4. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Supply voltage						
Vcc	Operating range after turn-on	$V_{COMP} > V_{COMPL}$	10.6		23	V
		$V_{COMP} = V_{COMPO}$	8		23	
Vcc_{On}	Turn-on threshold	(1)	13	14	15	V
Vcc_{Off}	Turn-off threshold	(1) $V_{COMP} > V_{COMPL}$	9.4	10	10.6	V
		(1) $V_{COMP} = V_{COMPO}$	7.2	7.6	8.0	
Hys	Hysteresis	$V_{COMP} > V_{COMPL}$		4		V
V_Z	Zener voltage	Icc = 20 mA, IC disabled	23	25	27	V
Supply current						
$I_{start-up}$	Startup current	Before turn-on, Vcc = 13 V		200	250	µA
I_q	Quiescent current	After turn-on, $V_{ZCD} = V_{CS}$ = 1 V		2.6	2.8	mA
Icc	Operating supply current	MODE/SC open		4	4.6	mA
I_{qdis}	Quiescent current	IC disabled (2)	330		2500	µA
		IC latched OFF		440	500	
High voltage startup generator						
V_{HV}	Breakdown voltage	(3) I_{HV} < 100 µA @ 25 °C	840			V
$V_{HVstart}$	Start voltage	I_{Vcc} < 100 µA	65	80	100	V
I_{charge}	Vcc charge current	$V_{HV} > V_{Hvstart}$, Vcc > 3 V	0.55	0.85	1	mA
$I_{HV, ON}$	ON-state current	$V_{HV} > V_{Hvstart}$, Vcc > 3 V			1.6	mA
		$V_{HV} > V_{Hvstart}$, Vcc = 0			0.8	
$I_{HV, OFF}$	OFF-state leakage current	V_{HV} = 400 V			40	µA
$V_{CCrestart}$	Vcc restart voltage	Vcc falling	4.4	5	5.6	V
		(1) IC latched OFF	12.5	13.5	14.5	
		(1) Disabled by $V_{COMP} < V_{COMPOFF}$	9.4	10	10.6	
Reference voltage						
V_{REF}	Output voltage	(1) T_J = 25 °C; I_{REF} = 1 mA	4.95	5	5.05	V
V_{REF}	Total variation	I_{REF} = 1 to 5 mA, Vcc = 10.6 to 23 V	4.9		5.1	V
I_{REF}	Short-circuit current	V_{REF} = 0	10		30	mA

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
	Sink capability in UVLO	Vcc = 6 V; Isink = 0.5 mA		0.2	0.5	V
V_{OV}	Overvoltage threshold		5.3	5.7		V
Internal oscillator						
f_{sw}	Oscillation frequency	Operating range	10		300	kHz
		T_J = 25 °C, V_{ZCD} = 0, MODE/SC = open	95	100	105	
		Vcc =12 to 23 V, V_{ZCD} = 0, MODE/SC = open	93	100	107	
V_{OSC}	Voltage reference	(4)	0.97	1	1.03	V
D_{max}	Maximum duty cycle	MODE/SC = open, V_{COMP} = 5 V	70		75	%
Brownout protection						
Vth	Threshold voltage	Voltage falling (turn-off)	0.432	0.450	0.468	V
		Voltage rising (turn-on)	0.452	0.485	0.518	V
I_{Hys}	Current hysteresis	Vcc > 5 V, V_{VFF} = 0.3 V	12	15	18	µA
$V_{AC_OK_CL}$	Clamp level	(1) I_{AC_OK} = 100 µA	3	3.15	3.3	V
Line voltage feedforward						
I_{VFF}	Input bias current	V_{VFF} = 0 to 3 V, $V_{ZCD} < V_{ZCDth}$			-1	µA
		$V_{ZCD} > V_{ZCDth}$	-0.7	-1		mA
V_{VFF}	Linear operation range			0 to 3		V
V_{OFF}	IC disable voltage		3	3.15	3.3	V
$V_{VFFlatch}$	Latch OFF/clamp level	$V_{ZCD} > V_{ZCDth}$		6.4		V
Kc	Control voltage gain (4)	V_{VFF} = 1 V, V_{COMP} = 4 V		0.4		V/V
K_{FF}	Feedforward gain (3)	V_{VFF} = 1 V, V_{COMP} = 4 V		0.04		V/V
Current sense comparator						
I_{CS}	Input bias current	V_{CS} = 0			-1	µA
t_{LEB}	Leading edge blanking		150	250	300	ns
$td_{(H-L)}$	Delay to output				100	ns
V_{CSx}	Overcurrent setpoint	$V_{COMP} = V_{COMPHI}$, V_{VFF} = 0 V	0.92	1	1.08	V
		$V_{COMP} = V_{COMPHI}$, V_{VFF} = 1.5 V	0.45	0.5	0.55	
		$V_{COMP} = V_{COMPHI}$, V_{VFF} = 3.0 V		0	0.1	
V_{CSdis}	Hiccup-mode OCP level	(1)	1.4	1.5	1.6	V
PWM control						
V_{COMPHI}	Upper clamp voltage	I_{COMP} = 0		5.7		V

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{COMPLO}	Lower clamp voltage	I_{SOURCE} = -1 mA		2.0		V
V_{COMPSH}	Linear dynamics upper limit	(1) V_{VFF} = 0 V	4.8	5	5.2	V
I_{COMP}	Max. source current	V_{COMP} = 3.3 V	320	400	480	µA
R_{COMP}	Dynamic resistance	V_{COMP} = 2.6 to 4.8 V		25		kΩ
V_{COMPBM}	Burst-mode threshold	(1)	2.52	2.65	2.78	V
		(1) MODE/SC = open	2.7	2.85	3	
Hys	Burst-mode hysteresis			20		mV
I_{CLAMPL}	Lower clamp capability	V_{COMP} = 2 V	-3.5		-1.5	mA
$V_{COMPOFF}$	Disable threshold	Voltage falling		1.4		V
V_{COMPO}	Level for lower UVLO OFF threshold (voltage falling)	(4)	2.61	2.75	2.89	V
		(4) MODE/SC = open	3.02	3.15	3.28	
V_{COMPL}	Level for higher UVLO OFF threshold (voltage rising)	(4)	2.9	3.05	3.2	V
		(4) MODE/SC = open	3.41	3.55	3.69	
Zero-current detector/overvoltage protection						
V_{ZCDH}	Upper clamp voltage	I_{ZCD} = 3 mA	5.4	5.7	6	V
V_{ZCDL}	Lower clamp voltage	I_{ZCD} = - 3 mA		-0.4		V
V_{ZCDA}	Arming voltage	(1) Positive-going edge	85	100	115	mV
V_{ZCDT}	Triggering voltage	(1) Negative-going edge	30	50	70	mV
I_{ZCD}	Internal pull-up	$V_{COMP} < V_{COMPSH}$			-1	µA
		V_{ZCD} < 2 V, $V_{COMP} = V_{COMPHI}$	-130	-100	-70	
I_{ZCDsrc}	Source current capability	$V_{ZCD} = V_{ZCDL}$	-3			mA
I_{ZCDsnk}	Sink current capability	$V_{ZCD} = V_{ZCDH}$	3			mA
T_{BLANK1}	Turn-on inhibit time	After gate-drive going low		2.5		µs
V_{ZCDth}	OVP threshold		4.85	5	5.15	V
T_{BLANK2}	OVP strobe delay	After gate-drive going low		2		µs
Latched shutdown function						
I_{OTP}	Input bias current	V_{DIS} = 0 to V_{OTP}			-1	µA
V_{OTP}	Disable threshold	(1)	4.32	4.5	4.68	V
Thermal shutdown						
Vth	Shutdown threshold			160		°C
Hys	Hysteresis			50		°C
External oscillator (frequency modulation)						
f_{FMOD}	Oscillation frequency	C_{MOD} = 0.1 µF	600	750	900	Hz
---	Usable frequency range		0.05		15	kHz

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{pk}	Peak voltage	(4)		1.5		V
V_{vy}	Valley voltage			0.5		V
I_{FMOD}	Charge/discharge current			150		µA
Mode selection / slope compensation						
$MODE_{th}$	Threshold for QR operation			3		V
SC_{pk}	Ramp peak (MODE/SC = open)	R_{S-COMP} = 3 kΩ to GND, GD pin HIGH, V_{COMP} = 5 V		1.7		V
SC_{vy}	Ramp starting value (MODE/SC = open)	R_{S-COMP} = 3 kΩ to GND, GD pin HIGH		0.3		V
	Ramp voltage (MODE/SC = open)	GD pin LOW		0		V
	Source capability (MODE/SC = open)	$V_{S-COMP} = V_{S-COMPpk}$	0.8			mA
Soft-start						
I_{SS1}	Charge current	T_J = 25 °C, V_{SS} < 2 V, V_{COMP} = 4 V	14	20	26	µA
I_{SS2}		T_J = 25 °C, V_{SS} > 2 V, $V_{COMP} = V_{COMPHi}$	3.5	5	6.5	
I_{SSdis}	Discharge current	V_{SS} > 2 V	3.5	5	6.5	µA
$V_{SSclamp}$	High saturation voltage	V_{COMP} = 4 V		2		V
V_{SSDIS}	Disable level	(1) $V_{COMP} = V_{COMPHi}$	4.85	5	5.15	V
V_{SSLAT}	Latch OFF level	$V_{COMP} = V_{COMPHi}$		6.4		V
Gate driver						
V_{GDH}	Output high voltage	$I_{GDsource}$ = 5 mA, Vcc = 12 V	9.8	11		V
V_{GDL}	Output low voltage	I_{GDsink} = 100 mA		0.75		V
$I_{sourcepk}$	Output source peak current		-0.6			A
I_{sinkpk}	Output sink peak current		0.8			A
t_f	Fall time			40		ns
t_r	Rise time			50		ns
$V_{GDclamp}$	Output clamp voltage	$I_{GDsource}$ = 5 mA; Vcc = 20 V	10	11.3	15	V
	UVLO saturation	Vcc = 0 to Vccon, I_{sink} = 1 mA		0.9	1.1	V

1. Parameters tracking one another.
2. See *Table 6 on page 18* and *Table 7 on page 44*.
3. For the thermal behavior, refer to *Figure 8*.
4. The voltage feedforward block output is given by:

$$V_{cs} = Kc\,(V_{COMP} - 2.5) - K_{FF}V_{VFF}$$

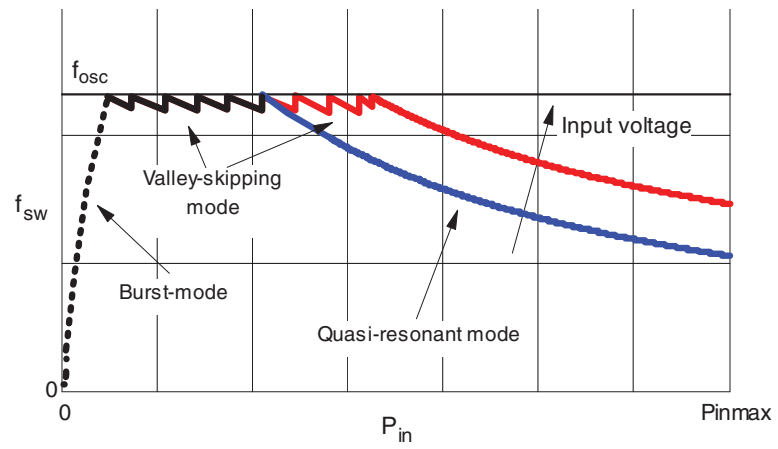
5 Application information

The L6566BH is a versatile peak-current-mode PWM controller specific to offline flyback converters. The device allows either fixed-frequency (FF) or quasi-resonant (QR) operation, selectable with the MODE/SC pin (12): forcing the voltage on the pin over 3 V (e.g. by tying it to the 5 V reference externally available at the VREF pin, 10) activates QR operation, otherwise the device is FF-operated.

Irrespective of the operating option selected by pin 12, the device is able to work in different modes, depending on the converter's load conditions. If QR operation is selected (see *Figure 4*):

1. QR mode at heavy load. Quasi-resonant operation lies in synchronizing MOSFET turn-on to the transformer's demagnetization by detecting the resulting negative-going edge of the voltage across any winding of the transformer. Then, the system works close to the boundary between discontinuous (DCM) and continuous conduction (CCM) of the transformer. As a result, the switching frequency is different for different line/load conditions (see the hyperbolic-like portion of the curves in *Figure 4*). Minimum turn-on losses, low EMI emission and safe behavior in short-circuit are the main benefits of this kind of operation.
2. Valley-skipping mode at medium/ light load. The externally programmable oscillator of the L6566BH, synchronized to MOSFET turn-on, enables the user to define the maximum operating frequency of the converter. As the load is reduced, MOSFET turn-on no longer occurs on the first valley but on the second one, the third one and so on. In this way the switching frequency no longer increases (piecewise linear portion in *Figure 4*).
3. Burst-mode with no or very light load. When the load is extremely light or disconnected, the converter enters a controlled on/off operation with constant peak current. Decreasing the load then results in frequency reduction, which can go down even to few hundred hertz, therefore minimizing all frequency-related losses and making it easier to comply with energy saving regulations or recommendations. With the peak current very low, no issue of audible noise arises.

Figure 4. Multimode operation with QR option active



If FF operation is selected:

1. FF mode from heavy to light load. The system operates exactly like a standard current mode control, at a frequency f_{sw} determined by the externally programmable oscillator: both DCM and CCM transformer operations are possible, depending on whether the power that it processes is greater or less than:

Equation 1

$$Pin_T = \frac{\left(\frac{Vin\ V_R}{Vin + V_R}\right)^2}{2 f_{sw}\ Lp}$$

where Vin is the input voltage to the converter, V_R the reflected voltage (i.e. the regulated output voltage times the primary-to-secondary turn ratio) and Lp the inductance of the primary winding. Pin_T is the power level that marks the transition from continuous to discontinuous operation mode of the transformer.

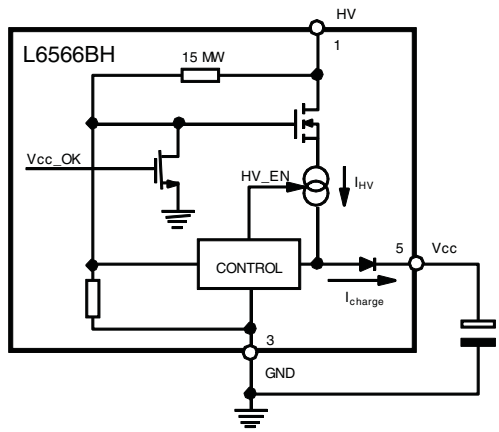
2. Burst-mode with no or very light load. This kind of operation is activated in the same way and results in the same behavior as previously described for QR operation.

The L6566BH is specifically designed for applications with no PFC front-end; pin 6 (F_{MOD}) features an auxiliary oscillator that can modulate the switching frequency (when FF operation is selected) in order to mitigate EMI emissions by a spread-spectrum action.

5.1 High voltage startup generator

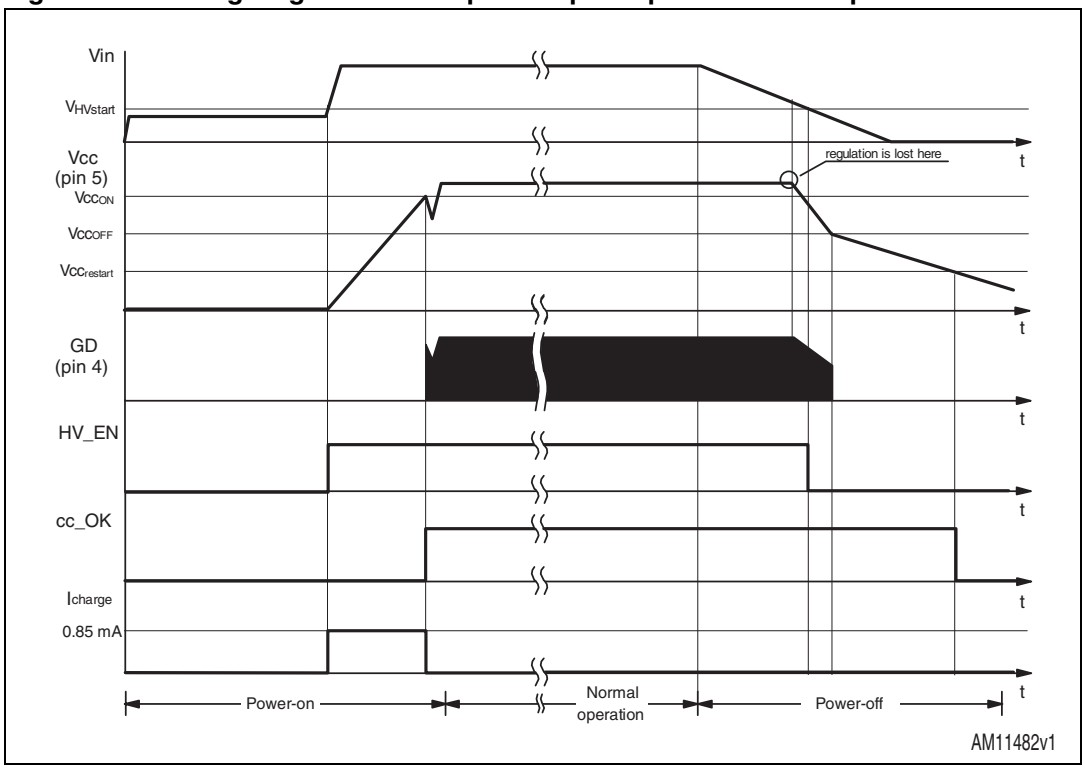
Figure 5 shows the internal schematic of the high voltage startup generator (HV generator). It is made up of a high voltage N-channel FET, whose gate is biased by a 15 MΩ resistor, with a temperature-compensated current generator connected to its source.

Figure 5. High voltage startup generator: internal schematic



With reference to the timing diagram of *Figure 6*, when power is first applied to the converter the voltage on the bulk capacitor (Vin) builds up and, at about 80 V, the HV generator is enabled to operate (HV_EN is pulled high) so that it draws about 1 mA. This current, minus the device consumption, charges the bypass capacitor connected from the Vcc pin (5) to ground and makes its voltage rise almost linearly.

Figure 6. Timing diagram: normal power-up and power-down sequences



As the Vcc voltage reaches the turn-on threshold (14 V typ.) the device starts operating and the HV generator is cut off by the Vcc_OK signal asserted high. The device is powered by the energy stored in the Vcc capacitor until the self-supply circuit (typically an auxiliary winding of the transformer and a steering diode) develops a voltage high enough to sustain the operation. The residual consumption of this circuit is just the one on the 15 MΩ resistor (≈ 10 mW at 400 Vdc), typically 50-70 times lower, under the same conditions, as compared to a standard startup circuit made with external dropping resistors.

At converter power-down the system loses regulation as soon as the input voltage is so low that either peak current or maximum duty cycle limitation is tripped. Vcc then drops and stops IC activity as it falls below the UVLO threshold (10 V typ.). The V_{CC}_OK signal is de-asserted as the Vcc voltage goes below a threshold V_{CCrest} located at about 5 V. The HV generator can now restart. However, if Vin < Vin_{start}, as illustrated in *Figure 6*, HV_EN is de-asserted too and the HV generator is disabled. This prevents converter restart attempts and ensures monotonic output voltage decay at power-down in systems where brownout protection (see the relevant section) is not used.

The low restart threshold V_{CCrest} ensures that, during short-circuits, the restart attempts of the device have a very low repetition rate, as shown in the timing diagram of *Figure 7*, and that the converter works safely with extremely low power throughput.

Figure 7. Timing diagram showing short-circuit behavior (SS pin clamped at 5 V)

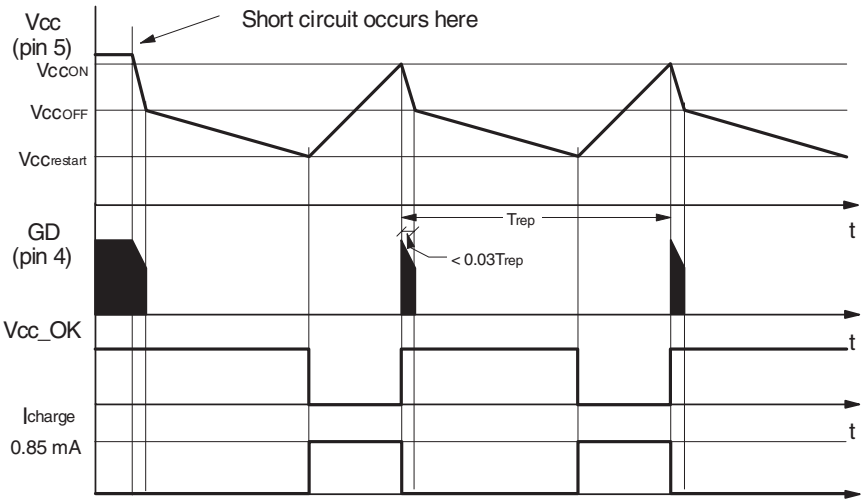
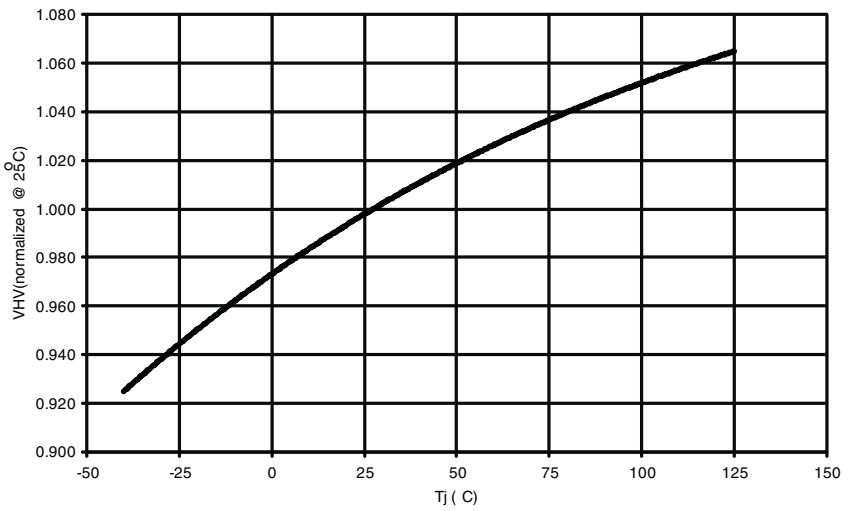


Figure 8. V_{HV} rating vs. temperature



5.2 Zero-current detection and triggering block; oscillator block

The zero-current detection (ZCD) and triggering blocks switch on the external MOSFET if a negative-going edge falling below 50 mV is applied to the input (pin 11, ZCD). To do so, the triggering block must be previously armed by a positive-going edge exceeding 100 mV.

This feature is typically used to detect transformer demagnetization for QR operation, where the signal for the ZCD input is obtained from the transformer's auxiliary winding used also to supply the L6566BH. The triggering block is blanked for T_{BLANK} = 2.5 µs after MOSFET

turn-off to prevent any negative-going edge that follows leakage inductance demagnetization from triggering the ZCD circuit erroneously.

The voltage at the pin is both top and bottom limited by a double clamp, as illustrated in the internal diagram of the ZCD block of *Figure 8*. The upper clamp is typically located at 5.7 V, while the lower clamp is located at -0.4 V. The interface between the pin and the auxiliary winding is a resistor divider. Its resistance ratio is properly chosen (see *Section 5.11: OVP block*) and the individual resistance values (R_{Z1}, R_{Z2}) are such that the current sourced and sunk by the pin is within the rated capability of the internal clamps (±3 mA).

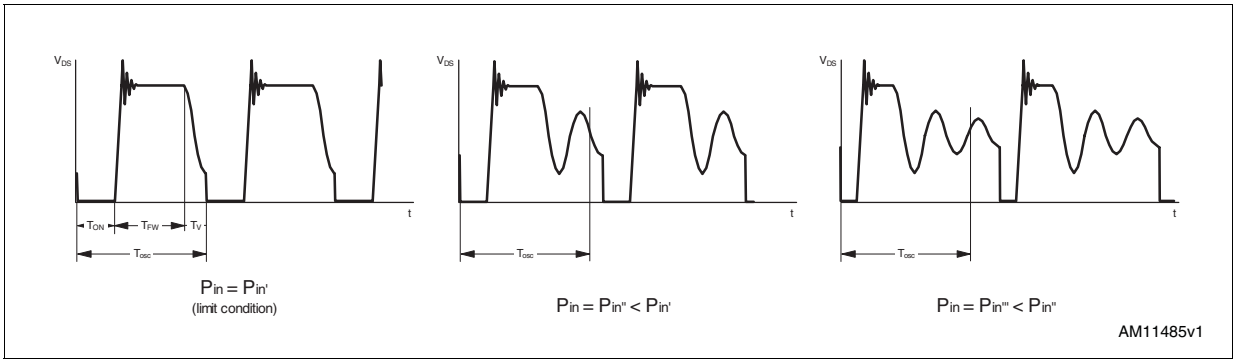
At converter power-up, when no signal is coming from the ZCD pin, the oscillator starts up the system. The oscillator is programmed externally by means of a resistor (R_T) connected from the OSC pin (13) to ground. With good approximation the oscillation frequency f_{osc} is:

Equation 2

$$f_{osc} \approx \frac{2 \cdot 10^3}{R_T}$$

(with f_{osc} in kHz and R_T in kΩ). As the device is turned on, the oscillator starts immediately; at the end of the first oscillator cycle, the voltage on the ZCD pin being zero, the MOSFET is turned on, therefore starting the first switching cycle right at the beginning of the second oscillator cycle. At any switching cycle, the MOSFET is turned off as the voltage on the current sense pin (CS, 7) hits an internal reference set by the line feedforward block, and the transformer starts demagnetization. If this completes (so a negative-going edge appears on the ZCD pin) after a time exceeding one oscillation period $T_{osc} = 1/f_{osc}$ from the previous turn-on, the MOSFET is turned on again – with some delay to ensure minimum voltage at turn-on – and the oscillator ramp is reset. If, on the other hand, the negative-going edge appears before T_{osc} has elapsed, it is ignored and only the first negative-going edge after T_{osc} turns on the MOSFET and synchronizes the oscillator. In this way one or more drain ringing cycles are skipped ("valley-skipping mode", *Figure 9*) and the switching frequency is prevented from exceeding f_{osc}.

Figure 9. Drain ringing cycle skipping as the load is gradually reduced



Note: When the system operates in valley skipping-mode, uneven switching cycles may be observed under some line/load conditions, due to the fact that the OFF-time of the MOSFET is allowed to change with discrete steps of one ringing cycle, while the OFF-time needed for cycle-by-cycle energy balance may fall in between. Therefore, one or more longer switching cycles is compensated by one or more shorter cycles and vice versa. However, this mechanism is absolutely normal and there is no appreciable effect on the performance of the converter or on its output voltage.

If the MOSFET is enabled to turn on but the amplitude of the signal on the ZCD pin is smaller than the arming threshold for some reason (e.g. a heavy damping of drain oscillations, like in some single-stage PFC topologies, or when a turn-off snubber is used), MOSFET turn-on cannot be triggered. This is identical to what happens at startup: at the end of the next oscillator cycle the MOSFET is turned on, and a new switching cycle takes place after skipping no more than one oscillator cycle.

The operation described so far does not consider the blanking time T_{BLANK} after MOSFET turn-off, and actually T_{BLANK} does not come into play as long as the following condition is met:

Equation 3

$$D \leq 1 - \frac{T_{BLANK}}{T_{osc}}$$

where D is the MOSFET duty cycle. If this condition is not met, there are no substantial changes: the time during which MOSFET turn-on is inhibited is extended beyond T_{osc} by a fraction of T_{BLANK}. As a consequence, the maximum switching frequency is a little lower than the programmed value f_{osc} and valley-skipping mode may take place slightly earlier than expected. However this is quite unusual: setting f_{osc} = 150 kHz, the phenomenon can be observed at duty cycles higher than 60%. See *Section 5.11: OVP block* for further implications of T_{BLANK}.

If the voltage on the COMP pin (9) saturates high, which reveals an open control loop, an internal pull-up keeps the ZCD pin close to 2 V during MOSFET OFF-time to prevent noise from false triggering the detection block. When this pull-up is active, the ZCD pin may not be able to go below the triggering threshold, which would stop the converter. To allow auto-restart operation, however ensuring minimum operating frequency in these conditions, the oscillator frequency that retriggers MOSFET turn-on is that of the external oscillator divided by 128. Additionally, to prevent malfunction at converter startup, the pull-up is disabled during the initial soft-start (see the relevant section). However, to ensure a correct startup, at the end of the soft-start phase the output voltage of the converter must meet the condition:

Equation 4

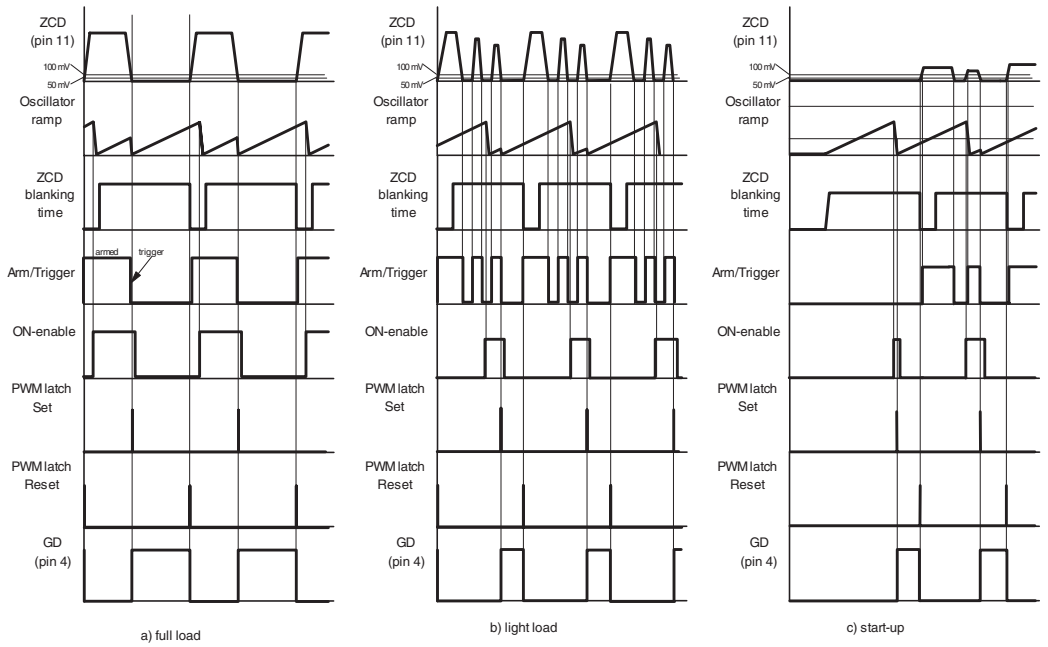
$$Vout > \frac{Ns}{Naux} R_{Z1} I_{ZCD}$$

where Ns is the turn number of the secondary winding, Naux the turn number of the auxiliary winding and I_{ZCD} the maximum pull-up current (130 µA).

The operation described so far under different operating conditions for the converter is illustrated in the timing diagrams of *Figure 10*.

If the FF option is selected the operation is exactly equal to that of a standard current-mode PWM controller. It works at a frequency fsw = fosc; both DCM and CCM transformer operations are possible, depending on the operating conditions (input voltage and output load) and on the design of the power stage. The MOSFET is turned on at the beginning of each oscillator cycle and is turned off as the voltage on the current sense pin reaches an internal reference set by the line feedforward block. The maximum duty cycle is limited to 70% minimum. The signal on the ZCD pin in this case is used only for detecting feedback loop failures (see *Section 5.11: OVP block*).

Figure 10. Operation of ZCD, triggering and oscillator blocks (QR option active)



5.3 Burst-mode operation at no load or very light load

When the voltage at the COMP pin (9) falls 20 mV below a threshold fixed internally at a value, V_{COMPBM}, depending on the selected operating mode, the L6566BH is disabled with the MOSFET kept in OFF-state and its consumption reduced to a lower value to minimize V_{CC} capacitor discharge.

The control voltage now increases as a result of the feedback reaction to the energy delivery stop (the output voltage is slowly decaying), the threshold is exceeded and the device restarts switching again. In this way the converter works in burst-mode with a nearly constant peak current defined by the internal disable level. A load decrease then causes a frequency reduction, which can go down even to few hundred hertz, therefore minimizing all frequency-related losses and making it easier to comply with energy saving regulations. This kind of operation, shown in the timing diagrams of *Figure 11* along with the others previously described, is noise-free since the peak current is low.

If it is necessary to decrease the intervention threshold of the burst-mode operation, this can be done by adding a small DC offset on the current sense pin as shown in *Figure 12*.

Note: The offset reduces the available dynamics of the current signal; thereby, the value of the sense resistor must be determined taking this offset into account.

Figure 11. Load-dependent operating modes: timing diagrams

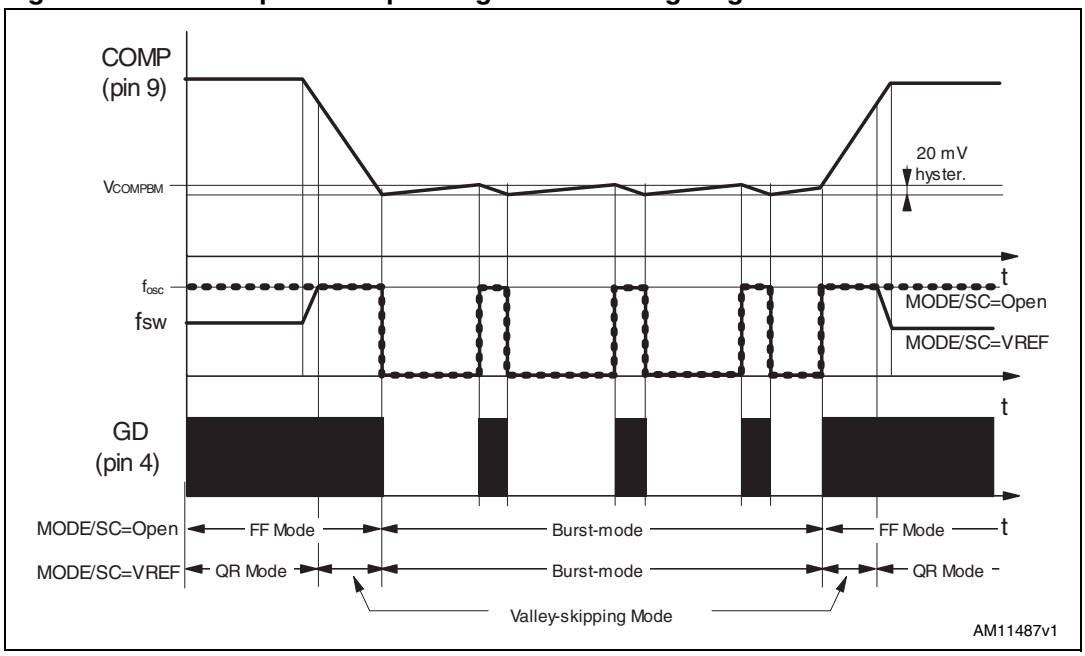
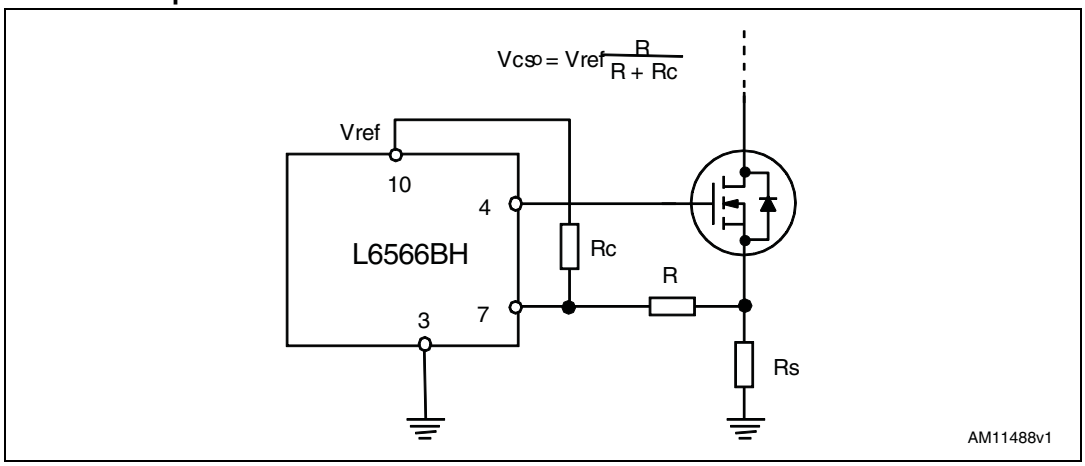


Figure 12. Addition of an offset to the current sense lowers the burst-mode operation threshold



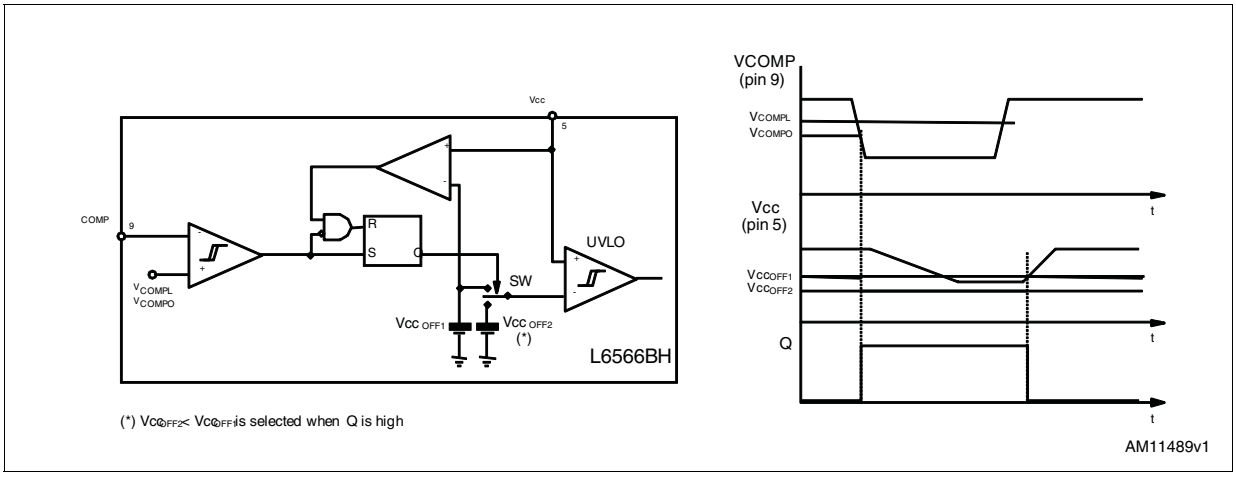
5.4 Adaptive UVLO

A major problem when optimizing a converter for minimum no-load consumption is that the voltage generated by the auxiliary winding under these conditions falls considerably as compared even to a few mA load. This very often causes the supply voltage Vcc of the control IC to drop and go below the UVLO threshold so that the operation becomes intermittent, which is undesired. Furthermore, this must be traded off against the need to generate a voltage not exceeding the maximum allowed by the control IC at full load.

To help the user overcome this problem, the device, besides reducing its own consumption during burst-mode operation, also features a proprietary adaptive UVLO function. It consists of shifting the UVLO threshold downwards at light load, namely when the voltage at the COMP pin falls below a threshold V_{COMPO} internally fixed, so as to have more headroom. To

prevent any malfunction during transients from minimum to maximum load the normal (higher) UVLO threshold is re-established when the voltage at the COMP pin exceeds V_{COMPL} and Vcc has exceeded the normal UVLO threshold (see *Figure 13*). The normal UVLO threshold ensures that at full load the MOSFET is driven with a proper gate-to-source voltage.

Figure 13. Adaptive UVLO block

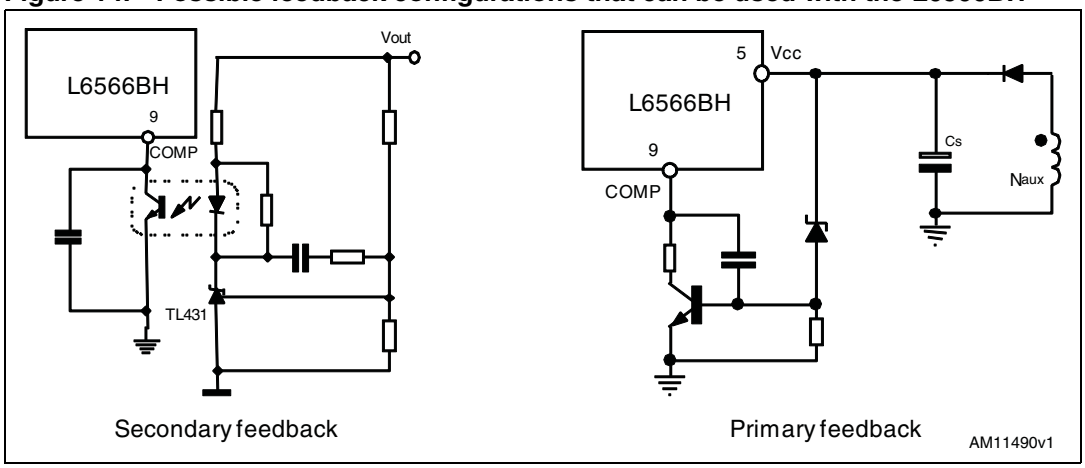


5.5 PWM control block

The device is specific to secondary feedback. Typically, there is a TL431 on the secondary side and an optocoupler that transfers output voltage information to the PWM control on the primary side, crossing the isolation barrier. The PWM control input (pin 9, COMP) is driven directly by the phototransistor's collector (the emitter is grounded to GND) to modulate the duty cycle (*Figure 14*, left-hand side circuit).

In applications where a tight output regulation is not required, it is possible to use a primary-sensing feedback technique. In this approach the voltage generated by the self-supply winding is sensed and regulated. This solution, shown in *Figure 14*, right-hand side circuit, is cheaper because no optocoupler or secondary reference is needed, but output voltage regulation, especially as a result of load changes, is quite poor.

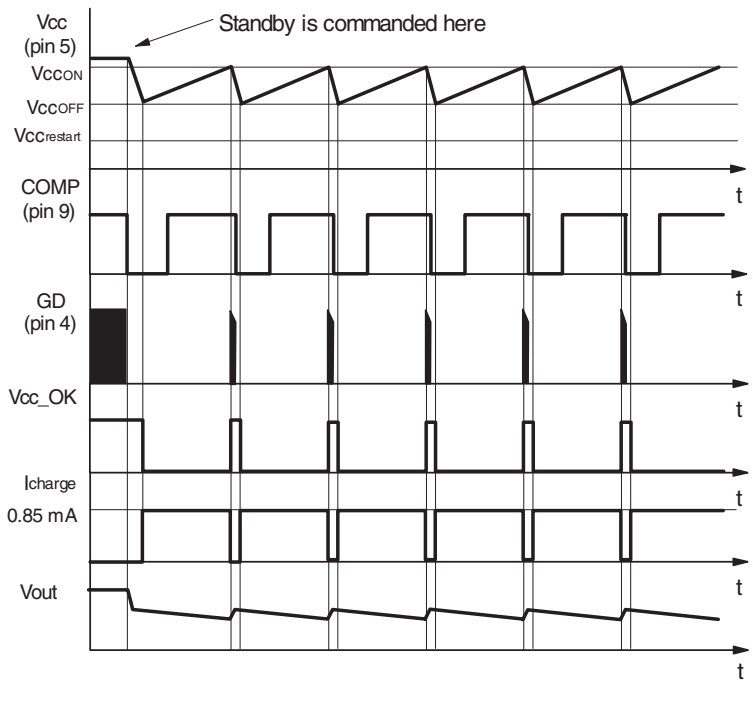
Figure 14. Possible feedback configurations that can be used with the L6566BH



Ideally, the voltage generated by the self-supply winding and the output voltage should be given by the relation between the Naux/Ns turn ratio only. Actually, numerous non-idealities, mainly transformer parasites, cause the actual ratio to deviate from the ideal one. Line regulation is quite good, in the range of ± 2%, whereas load regulation is about ± 5% and output voltage tolerance is in the range of ± 10%.

The dynamics of the pin are in the 2.5 to 5 V range. The voltage at the pin is clamped downwards at about 2 V. If the clamp is externally overridden and the voltage on the pin is pulled below 1.4 V, the L6566BH shuts down. This condition is latched as long as the device is supplied. While the device is disabled, however, no energy is coming from the self-supply circuit, therefore the voltage on the Vcc capacitor decays and crosses the UVLO threshold after some time, which clears the latch and lets the HV generator restart. This function is intended for an externally controlled burst-mode operation at light load with a reduced output voltage, a technique typically used in multi-output SMPS, such as those for TVs or monitors (see the timing diagram *Figure 15*).

Figure 15. Externally controlled burst-mode operation by driving the COMP pin: timing diagram



5.6 PWM comparator, PWM latch and voltage feedforward blocks

The PWM comparator senses the voltage across the current sense resistor Rs and, by comparing it to the programming signal delivered by the feedforward block, determines the exact time when the external MOSFET is to be switched off. Its output resets the PWM latch, previously set by the oscillator or the ZCD triggering block, which asserts the gate driver output low. The use of PWM latch avoids spurious switching of the MOSFET that may result from the noise generated (“double-pulse suppression”).

Cycle-by-cycle current limitation is realized with a second comparator (OCP comparator) that senses the voltage across the current sense resistor Rs as well and compares this voltage to a reference value V_{CSX}. Its output is OR-ed with that of the PWM comparator (see the circuit schematic in *Figure 17*). In this way, if the programming signal delivered by the feedforward block and sent to the PWM comparator exceeds V_{CSX}, it is the OCP comparator to reset first the PWM latch instead of the PWM comparator. The value of V_{csx}, thereby, determines the overcurrent setpoint along with the sense resistor Rs.

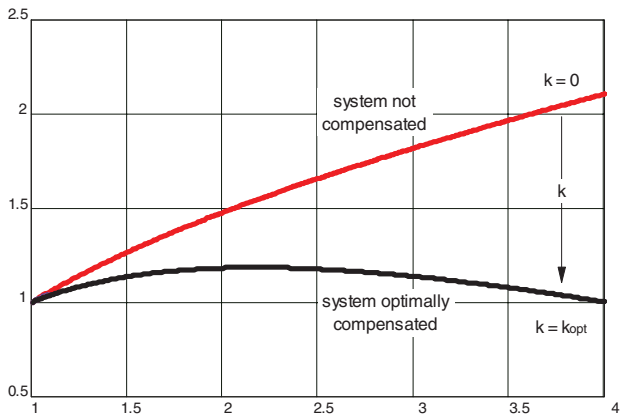
The power that QR flyback converters with a fixed overcurrent setpoint (like fixed-frequency systems) are able to deliver changes considerably with the input voltage. With wide-range mains, at maximum line it can be more than twice the value at minimum line, as shown by the upper curve in the diagram of *Figure 16*. The device has the line feedforward function available to solve this issue.

It acts on the overcurrent setpoint V_{CSX}, so that it is a function of the converter's input voltage Vin sensed through a dedicated pin (15, VFF): the higher the input voltage, the lower the setpoint. This is illustrated in the diagram on the left-hand side of *Figure 17*: it shows the relationship between the voltage on the pin VFF and V_{CSX} (with the error amplifier saturated high in the attempt to obtain output voltage regulation):

Equation 5

$$V_{csx} = 1 - \frac{V_{VFF}}{3} = 1 - \frac{k}{3} Vin$$

Figure 16. Typical power capability change vs. input voltage in QR flyback converters



Note: If the voltage on the pin exceeds 3 V, switching ceases but the soft-start capacitor is not discharged. The schematic in Figure 17 shows also how the function is included in the control loop.

With a proper selection of the external divider R1-R2, i.e. of the ratio k = R2 / (R1+R2), it is possible to achieve the optimum compensation described by the lower curve in the diagram of *Figure 16*.

The optimum value of k, k_{opt}, which minimizes the power capability variation over the input voltage range, is the one that provides equal power capability at the extremes of the range. The exact calculation is complex, and non-idealities shift the real-world optimum value from

the theoretical one. It is therefore more practical to provide a first cut value, simple to calculate, and then to fine tune experimentally.

Assuming that the system operates exactly at the boundary between DCM and CCM, and neglecting propagation delays, the following expression for k_{opt} can be found:

Equation 6

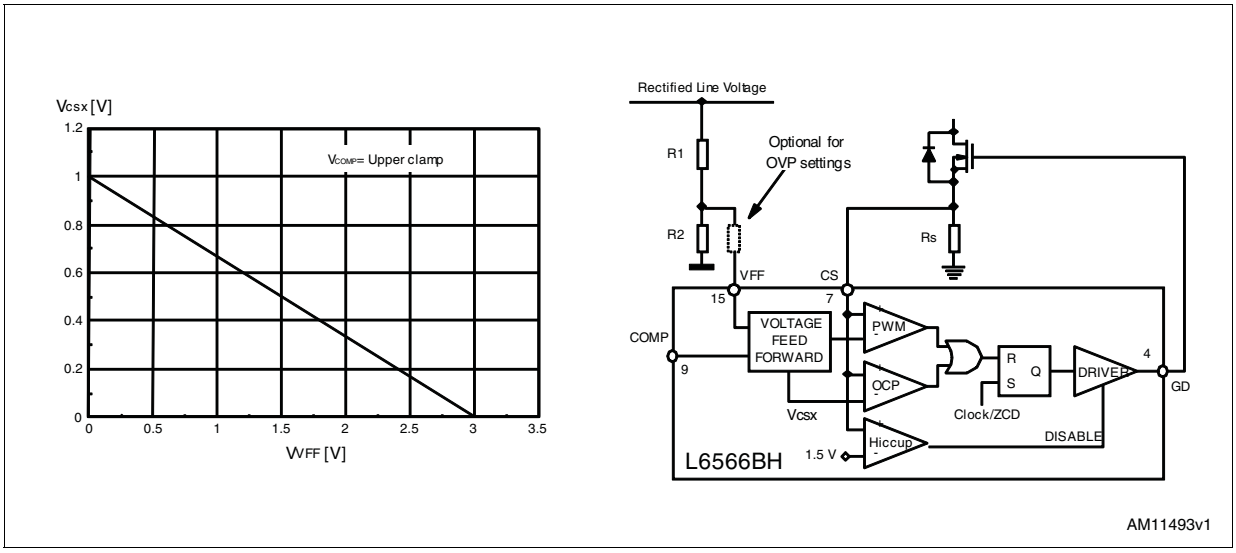
$$k_{opt} = 3 \cdot \frac{V_R}{V_{in\,min} \cdot V_{in\,max} + \left(V_{in\,min} + V_{in\,max}\right) \cdot V_R}$$

Experience shows that this value is typically lower than the real one. Once the maximum peak primary current, I_{PKpmax}, occurring at minimum input voltage Vin_{min} has been found, the value of Rs can be determined from (5):

Equation 7

$$Rs = \frac{1 - \frac{k_{opt}}{3} V_{in\,min}}{I_{PKp\,max}}$$

Figure 17. Left: overcurrent setpoint vs. VFF voltage; right: line feedforward function block



The converter is then tested on the bench to find the output power level $Pout_{lim}$ where regulation is lost (because overcurrent is being tripped) both at Vin = Vin_{min} and Vin = Vin_{max}.

If $Pout_{lim}$ @ Vin_{max} > $Pout_{lim}$ @ Vin_{min} the system is still undercompensated and k needs to increase; if $Pout_{lim}$ @ Vin_{max} < $Pout_{lim}$ @ Vin_{min} the system is overcompensated and k needs to decrease. This goes on until the difference between the two values is acceptably low. Once the true k_{opt} is found in this way, it is possible that $Pout_{lim}$ can turn out slightly different from the target; to correct this, the sense resistor Rs needs to be adjusted and the above tuning process is repeated with the new Rs value. Typically, a satisfactory setting is achieved in no more than a couple of iterations.

In applications where this function is not wanted, e.g. because of a narrow input voltage range, the VFF pin can be simply grounded, directly or through a resistor, depending on whether the user wants the OVP function to be auto-restart or latched mode (see "*Section 5.11: OVP block*"). The overcurrent setpoint is then fixed at the maximum value of 1 V. If a lower setpoint is desired to reduce the power dissipation on Rs, the pin can be also biased at a fixed voltage using a divider from VREF (pin 10).

If the FF option is selected the line feedforward function can be still used to compensate for the total propagation delay Td of the current sense chain (internal propagation delay $td_{(H-L)}$ plus the turn-off delay of the external MOSFET), which in standard current mode PWM controllers is done by adding an offset on the current sense pin proportional to the input voltage. In that case the divider ratio k, which is much smaller as compared to that used with the QR option selected, can be calculated with the following equation:

Equation 8

$$k_{opt} = 3\frac{Td}{Rs\,Lp}$$

where Lp is the inductance of the primary winding. In case a constant maximum power capability vs. the input voltage is not required, the VFF pin can be grounded, directly or through a resistor (see *Section 5.11: OVP block*), therefore fixing the overcurrent setpoint at 1 V, or biased at a fixed voltage through a divider from VREF to obtain a lower setpoint.

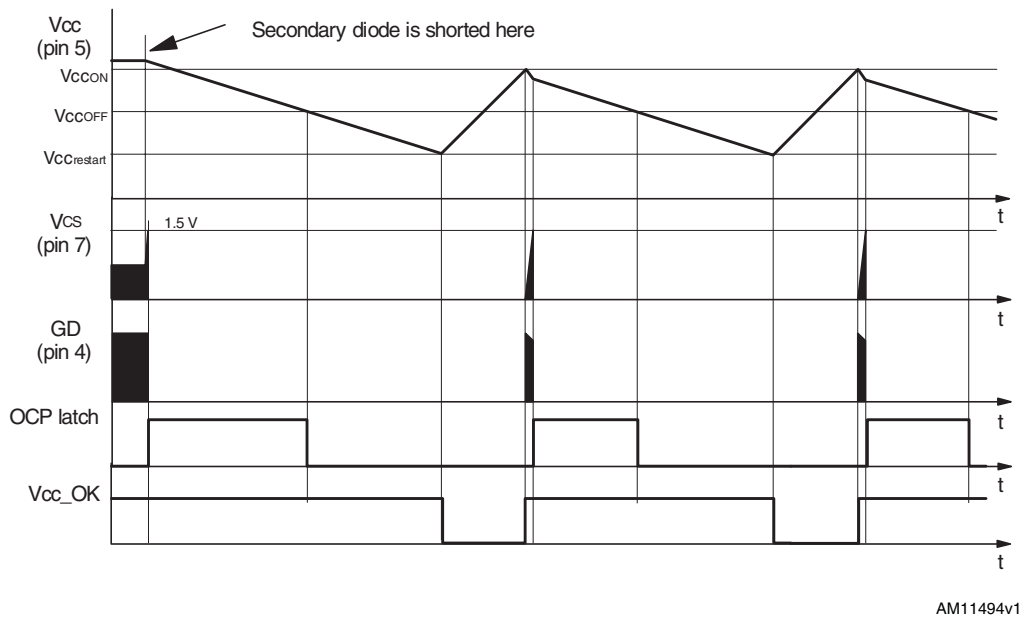
It is possible to bypass the pin to ground with a small film capacitor (e.g. 1-10 nF) to ensure a clean operation of the IC even in a noisy environment.

The pin is internally forced to ground during UVLO, after activating any latched protection and when the COMP pin is pulled below its low clamp voltage (see *Section 5.5: PWM control block*).

5.7 Hiccup-mode OCP

A third comparator senses the voltage on the current sense input and shuts down the device if the voltage on the pin exceeds 1.5 V, a level well above that of the maximum overcurrent setpoint (1 V). Such an anomalous condition is typically generated by either a short-circuit of the secondary rectifier or a shorted secondary winding or a hard-saturated flyback transformer.

Figure 18. Hiccup-mode OCP: timing diagram



To distinguish an actual malfunction from a disturbance (e.g. induced during ESD tests), the first time the comparator is tripped the protection circuit enters a “warning state”. If in the next switching cycle the comparator is not tripped, a temporary disturbance is assumed and the protection logic is reset in its idle state; if the comparator is again tripped, a real malfunction is assumed and the L6566BH is stopped. Depending on the time relationship between the detected event and the oscillator, the device may occasionally stop after the third detection.

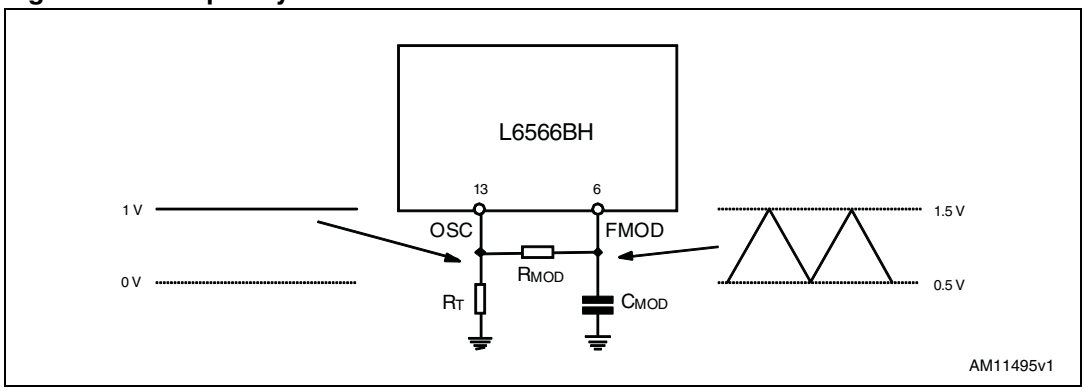
This condition is latched as long as the device is supplied. While it is disabled, however, no energy comes from the self-supply circuit; hence the voltage on the V_{CC} capacitor decays and crosses the UVLO threshold after some time, which clears the latch. The internal startup generator is still off, and the V_{CC} voltage still needs to go below its restart voltage before the V_{CC} capacitor is charged again and the device restarted. Ultimately, this results in a low-frequency intermittent operation (Hiccup-mode operation), with very low stress on the power circuit. This special condition is illustrated in the timing diagram of *Figure 18*.

5.8 Frequency modulation

To alleviate the converter’s EMI emissions and reduce cost and size of the line filter, it is advantageous to modulate its switching frequency, so that the resulting spread-spectrum action distributes the energy of each harmonic of the switching frequency over a number of side-band harmonics. Their overall energy is unchanged but the individual amplitudes are smaller. This is what naturally occurs with QR operation, due to the twice-mains-frequency ripple appearing on the input bulk capacitor, which translates into different DCM-CCM boundary frequencies.

The L6566BH is provided with a dedicated pin, F_{MOD} (6), to perform this function if FF mode is selected.

Figure 19. Frequency modulation circuit



With reference to *Figure 19*, the capacitor C_{MOD} is connected from F_{MOD} to ground and is alternately charged and discharged between 0.5 and 1.5 V by internal current generators sourcing and sinking the same current (three times the current defined by the resistor R_T on pin OSC). Therefore, the voltage across C_{MOD} is a symmetric triangle, whose frequency f_m is determined by C_{MOD}. By connecting a resistor R_{MOD} from R_{MOD} to OSC, the current sourced by the OSC pin is modulated according to a triangular profile at a frequency f_m. If R_{MOD} is considerably higher than R_T, as is normal, both f_m and the symmetry of the triangle is little affected.

With this arrangement it is possible to set, nearly independently, the frequency deviation Δf_{sw} and the modulating frequency f_m, which define the modulation index:

Equation 9

$$\beta = \frac{\Delta f_{sw}}{f_m}$$

which is the parameter that the amplitude of the generated side-band harmonics depends on.

The minimum frequency f_{sw_min} (occurring on the peak of the triangle) and the maximum frequency f_{sw_max} (occurring on the valley of the triangle) is symmetrically placed around the centre value f_{sw}, so that:

Equation 10

$$f_{sw_min} = f_{sw} - \tfrac{1}{2}\Delta f_{sw}\,; \qquad f_{sw_max} = f_{sw} + \tfrac{1}{2}\Delta f_{sw}$$

Then, R_T is found from (5) (see *Section 5.2: Zero-current detection and triggering block; oscillator block*), while R_{MOD} and C_{MOD} can be calculated as follows:

Equation 11

$$R_{MOD} = \frac{2 \cdot 10^3}{\Delta f_{sw}} \qquad C_{MOD} = \frac{75}{f_m}$$

where Δf_{sw} and f_m (in kHz, with C_{MOD} in nF and R_{MOD} in kΩ) are selected by the user as to achieve the best compromise between attenuation of peak EMI emissions and clean converter operation.

5.9 Latched disable function

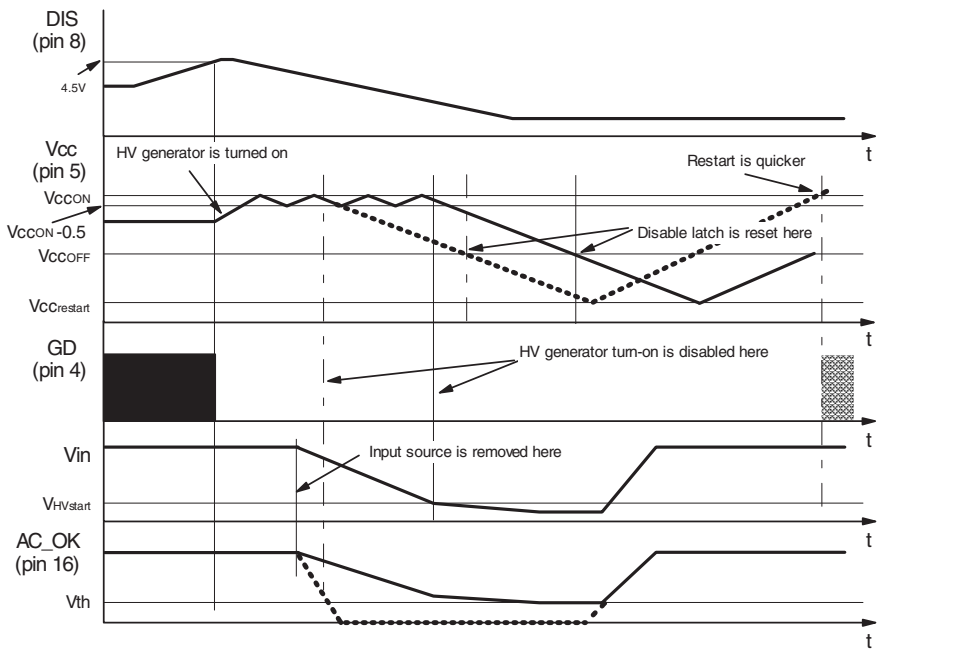
The device is equipped with a comparator having the non-inverting input externally available at the pin DIS (8) and with the inverting input internally referenced to 4.5 V. As the voltage on the pin exceeds the internal threshold, the device is immediately shut down and its consumption reduced to a low value.

The information is latched and it is necessary to let the voltage on the Vcc pin go below the UVLO threshold to reset the latch and restart the device. To keep the latch supplied as long as the converter is connected to the input source, the HV generator is activated periodically so that Vcc oscillates between the startup threshold V_{CCON} and V_{ccON} - 0.5 V. Activating the HV generator in this way cuts its power dissipation approximately by three (as compared to continuous conduction) and keeps peak silicon temperature close to the average value.

To let the L6566BH restart, it is then necessary to disconnect the converter from the input source. Pulling pin 16 (AC_OK) below the disable threshold (see *Section 5.12: Brownout protection*) stops the HV generator until Vcc falls below $V_{CCrestart}$, so that the latch can be cleared and a quicker restart is allowed as the input source is removed. This operation is shown in the timing diagram of *Figure 20*.

This function is useful in order to implement a latched overtemperature protection very easily by biasing the pin with a divider from VREF, where the upper resistor is an NTC physically located close to a heating element like the MOSFET, or the transformer. The DIS pin is a high impedance input, therefore it is prone to pick-up noise, which may lead to undesired latch OFF of the device. It is possible to bypass the pin to ground with a small film capacitor (e.g. 1-10 nF) to prevent any malfunctioning of this kind.

Figure 20. Operation after latched disable activation: timing diagram



5.10 Soft-start and delayed latched shutdown upon overcurrent

At device startup, a capacitor (C_{SS}) connected between the SS pin (14) and ground is charged by an internal current generator, I_{SS1}, from zero up to about 2 V where it is clamped. During this ramp, the overcurrent setpoint progressively rises from zero to the value imposed by the voltage on the VFF pin (15, see *Section 5.6: PWM comparator, PWM latch and voltage feedforward blocks*); MOSFET conduction time increases gradually, therefore controlling the startup inrush current. The time needed for the overcurrent setpoint to reach its steady-state value, referred to as soft-start time, is approximately:

Equation 12

$$T_{SS} = \frac{Css}{I_{SS1}} V_{csx}(V_{VFF}) = \frac{Css}{I_{SS1}}\left(1 - \frac{V_{VFF}}{3}\right)$$

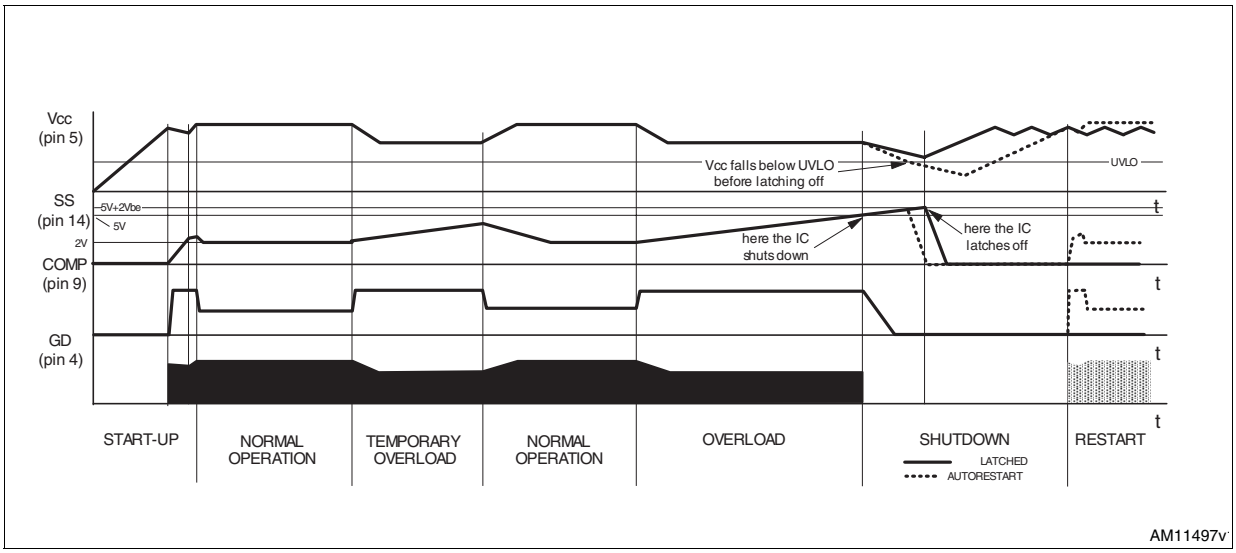
During the ramp (i.e. until $V_{SS} = 2$ V) all the functions that monitor the voltage on the COMP pin are disabled.

The soft-start pin is also invoked whenever the control voltage (COMP) saturates high, which reveals an open loop condition for the feedback system. This condition very often occurs at startup, but may be also caused by either a control loop failure or a converter overload/short-circuit. A control loop failure results in an output overvoltage that is handled by the OVP function of the L6566BH (see next section). In the case of QR operation, a short-circuit causes the converter to run at a very low frequency, then with very low power capability. This makes the self-supply system that powers the device unable to keep it operating, so that the converter works intermittently, which is very safe. In the case of

overload, the system has a power capability lower than that at nominal load but the output current may be quite high and can overstress the output rectifier. In the case of FF operation the capability is almost unchanged and both short-circuit and overload conditions are more critical to handle.

The L6566BH, regardless of the operating option selected, makes it easier to handle such conditions: the 2 V clamp on the SS pin is removed and a second internal current generator $I_{SS2} = I_{SS1}/4$ continues to charge C_{SS}. As the voltage reaches 5 V the device is disabled, if it is allowed to reach 2 V_{BE} over 5 V, the device is latched off. In the former case the resulting behavior is identical to that of short-circuit illustrated in *Figure 7*; in the latter case the result is identical to that of *Figure 20*. See *Section 5.9: Latched disable function* for additional details.

Figure 21. Soft-start pin operation under different operating conditions and settings



A diode, with the anode to the SS pin and the cathode connected to the VREF pin (10), is the simplest way to select either auto-restart mode or latch-mode behavior upon overcurrent. If the overload disappears before the Css voltage reaches 5 V, the I_{SS2} generator is turned off and the voltage gradually brought back down to 2 V. Refer to *Section 6: Application examples and ideas* (*Table 7*) for additional information.

If latch-mode behavior is desired also for converter short-circuit, make sure that the supply voltage of the device does not fall below the UVLO threshold before activating the latch. *Figure 21* shows soft-start pin behavior under different operating conditions and with different settings (latch-mode or auto-restart).

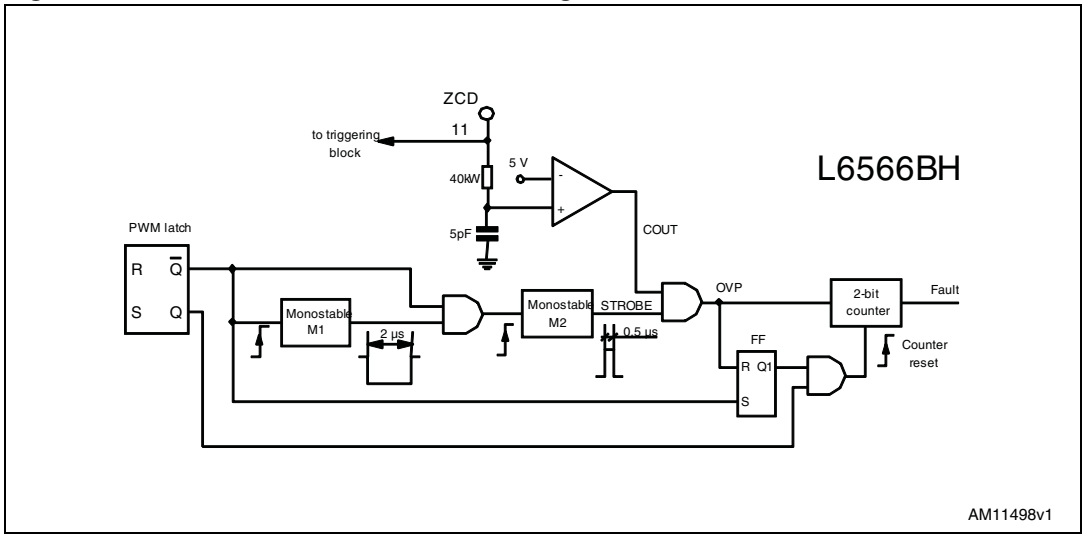
Note: Unlike other PWM controllers provided with a soft-start pin, in the L6566BH grounding the SS pin does not guarantee that the gate driver is disabled.

5.11 OVP block

The OVP function of the L6566BH monitors the voltage on the ZCD pin (11) in MOSFET OFF-time, during which the voltage generated by the auxiliary winding tracks the converter's output voltage. If the voltage on the pin exceeds an internal 5 V reference, a comparator is triggered, an overvoltage condition is assumed and the device is shut down. An internal current generator is activated that sources 1 mA out of the VFF pin (15). If the VFF voltage

is allowed to reach 2 Vbe over 5 V, the L6566BH is latched off. See *Section 5.9: Latched disable function* for more details on IC behavior under these conditions. If the impedance externally connected to pin 15 is so low that the 5+2 V_{BE} threshold cannot be reached or if some means is provided to prevent that, the device is able to restart after the Vcc has dropped below 5 V. Refer to *Section 6: Application examples and ideas* (*Table 7*) for additional information.

Figure 22. OVP function: internal block diagram



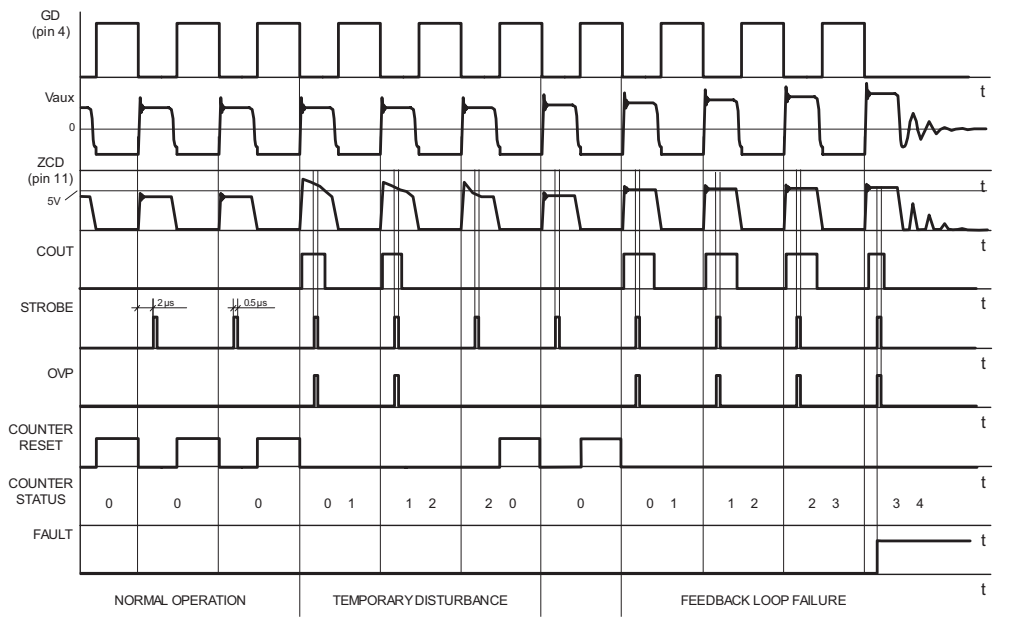
The ZCD pin is connected to the auxiliary winding through a resistor divider R_{Z1}, R_{Z2} (see *Figure 8*). The divider ratio $k_{OVP} = R_{Z2} / (R_{Z1} + R_{Z2})$ is chosen equal to:

Equation 13

$$k_{OVP} = \frac{5}{Vout_{OVP}} \frac{Ns}{Naux}$$

where $Vout_{OVP}$ is the output voltage value that is to activate the protection, Ns the turn number of the secondary winding, and Naux the turn number of the auxiliary winding.

Figure 23. OVP function: timing diagram



The value of R_{Z1} is such that the current sourced by the ZCD pin be within the rated capability of the internal clamp:

Equation 14

$$R_{Z1} \geq \frac{1}{3 \cdot 10^{-3}} \frac{Naux}{Np} Vin_{max}$$

where Vin_{max} is the maximum DC input voltage and Ns the turn number of the primary winding. See *Section 5.2: Zero-current detection and triggering block; oscillator block* for additional details.

To reduce sensitivity to noise and prevent the latch from being erroneously activated, firstly the OVP comparator is active only for a small time frame (typically, 0.5 µs) starting 2 µs after MOSFET turn-off, to reject the voltage spike associated to the positive-going edges of the voltage across the auxiliary winding Vaux; secondly, to stop the L6566BH, the OVP comparator must be triggered for four consecutive switching cycles. A counter, which is reset every time the OVP comparator is not triggered in one switching cycle, is provided for this purpose.

Figure 22 shows the internal block diagram, while the timing diagrams in *Figure 23* illustrate the operation.

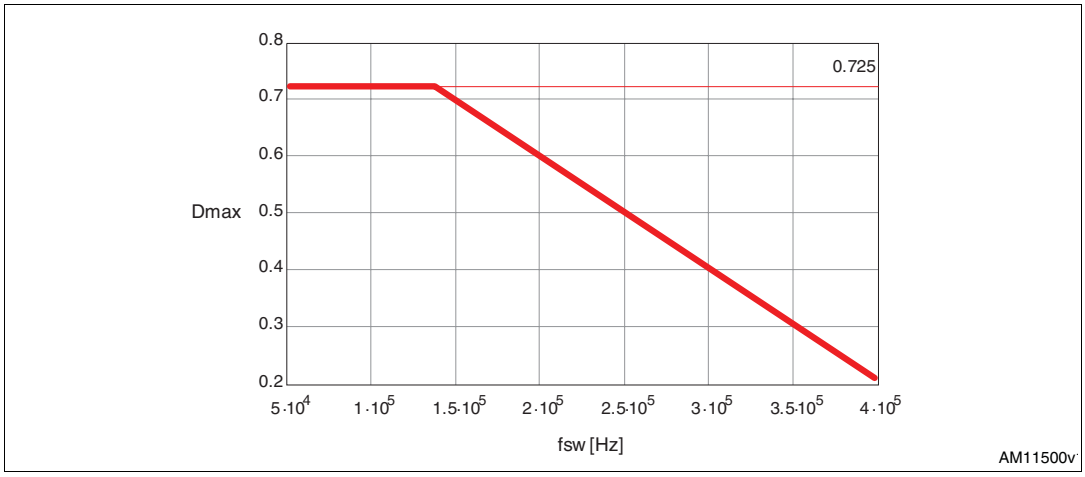
Note: To use the OVP function effectively, i.e. to ensure that the OVP comparator is always interrogated during MOSFET OFF-time, the duty cycle D under open loop conditions must fulfill the following inequality:

Equation 15

$$D + T_{BLANK2}\, f_{sw} \leq 1$$

where T_{BLANK2} = 2 µs; this is also illustrated in the diagram of *Figure 24*.

Figure 24. Maximum allowed duty cycle vs. switching frequency for correct OVP detection



5.12 Brownout protection

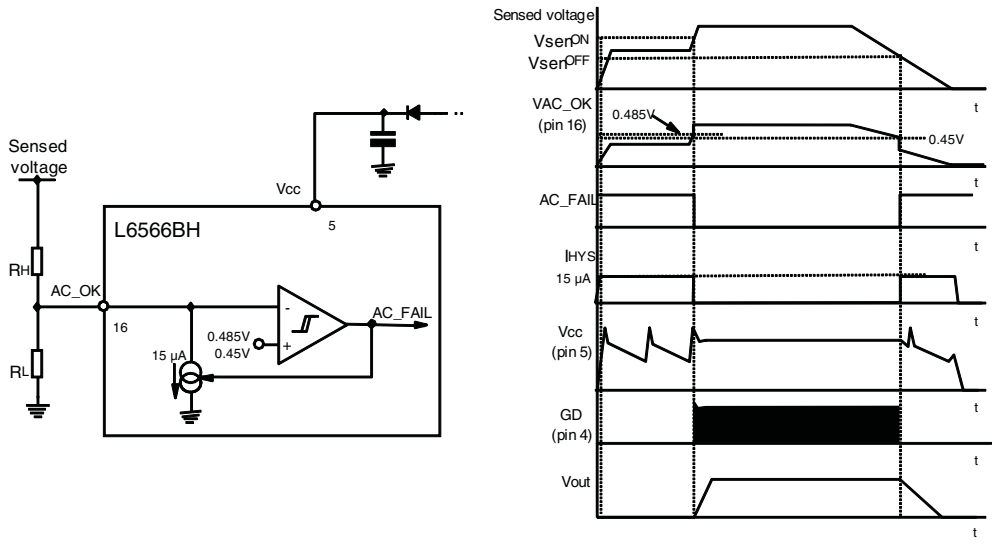
Brownout protection is basically a not-latched device shutdown function activated when a condition of mains undervoltage is detected. There are several reasons why it may be desirable to shut down a converter during a brownout condition, which occurs when the mains voltage falls below the minimum specification of normal operation.

Firstly, a brownout condition may cause overheating of the primary power section due to an excess of RMS current. Secondly, spurious restarts may occur during converter power down, therefore causing the output voltage to not decay to zero monotonically.

L6566BH shutdown upon brownout is accomplished by means of an internal comparator, as shown in the block diagram of *Figure 25*, which shows the basic usage. The inverting input of the comparator, available on the AC_OK pin (16), is supposed to sense a voltage proportional to the RMS (peak) mains voltage; the non-inverting input is internally referenced to 0.485 V with 35 mV hysteresis. If the voltage applied on the AC_OK pin before the device starts operating does not exceed 0.485 V or if it falls below 0.45 V while the device is running, the AC_FAIL signal goes high and the device shuts down, with the soft-start capacitor discharged and the gate-drive output low. Additionally, if the device has been latched off by some protection function (testified by Vcc oscillating between V_{CCON} and V_{CCON} - 0.5 V) the AC_OK voltage falling below 0.45 V clears the latch. This may allow a quicker restart as the input source is removed.

While the brownout protection is active the startup generator keeps on working but, there being no PWM activity, the Vcc voltage continuously oscillates between the startup and the HV generator restart thresholds, as shown in the timing diagram of *Figure 25*.

Figure 25. Brownout protection: internal block diagram and timing diagram



The brownout comparator is provided with current hysteresis in addition to voltage hysteresis: an internal 15 µA current sink is ON as long as the voltage applied on the AC_OK pin is such that the AC_FAIL signal is high. This approach provides an additional degree of freedom: it is possible to set the ON threshold and the OFF threshold separately by properly choosing the resistors of the external divider (see below). With just voltage hysteresis, on the other hand, fixing one threshold automatically fixes the other one depending on the built-in hysteresis of the comparator.

With reference to *Figure 25*, the following relationships can be established for the ON ($Vsen_{ON}$) and OFF ($Vsen_{OFF}$) thresholds of the sensed voltage:

Equation 16

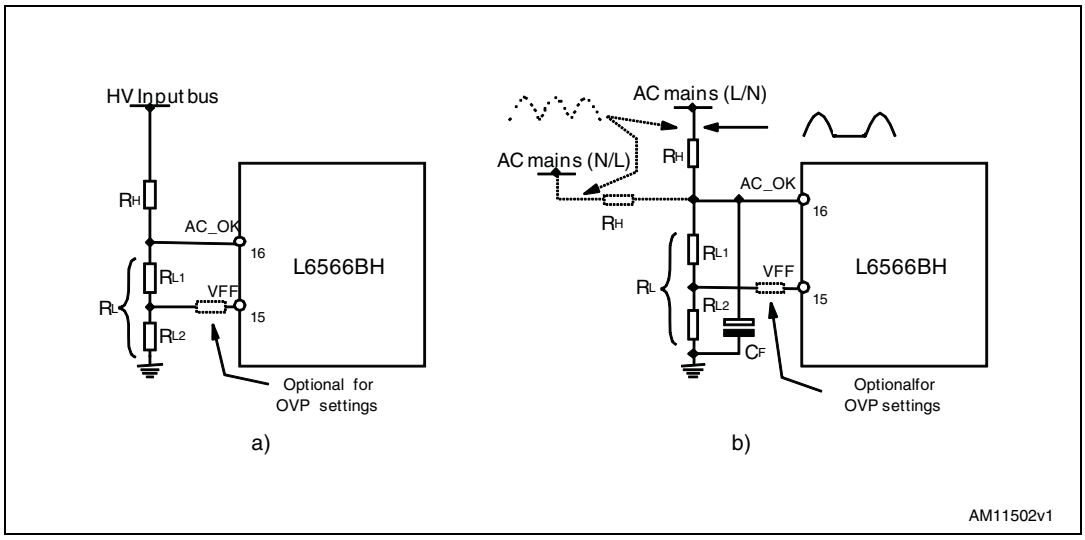
$$\frac{Vsen_{ON} - 0.485}{R_H} = 15 \cdot 10^{-6} + \frac{0.485}{R_L} \qquad \frac{Vsen_{OFF} - 0.45}{R_H} = \frac{0.45}{R_L}$$

which, solved for R_H and R_L, yields:

Equation 17

$$R_H = \frac{Vsen_{ON} - 1.078 \cdot Vsen_{OFF}}{15 \cdot 10^{-6}}; \qquad R_L = R_H \frac{0.45}{Vsen_{OFF} - 0.45}$$

Figure 26. Voltage sensing techniques to implement brownout protection with the L6566BH



It is usually convenient to use a single divider to bias both the AC_OK and the VFF pins, as shown in *Figure 26*: this is possible because in all practical cases the voltage on the VFF pin is lower than that on the AC_OK pin. Once R_H and R_L have been found, as suggested above, and k_{opt}, either calculated from (6) or (8) or experimentally found, R_L is split as:

Equation 18

$$R_{L2} = k_{opt}\left(R_L + R_H\right) \quad ; \quad R_{L1} = R_L - R_{L2}$$

Circuit a) senses the input voltage bus (across the bulk capacitor, downstream of the bridge rectifier); in this case, for a proper operation of the brownout function, $Vsen_{ON}$ must be lower than the peak voltage at minimum mains and $Vsen_{OFF}$ lower than the minimum voltage on the input bulk capacitor at minimum mains and maximum load considering, if necessary, holdup requirements during mains missing cycles as well. Brownout level is load-dependent. In case of latched shutdown, when the input source is removed it is necessary to wait until the bulk capacitor voltage falls below the start voltage of the HV generator $V_{HVstart}$ in order for the unit to restart, which may take up to several seconds.

Circuit b) senses the mains voltage directly, upstream of the bridge rectifier. It can be configured either for half-wave sensing (only the line/neutral wire is sensed) or full-wave sensing (both neutral and line are sensed); in the first case, assuming C_F is large enough, the sensed voltage is equal to $1/\pi$ the peak mains voltage, while in the second case it is equal to $2/\pi$ the peak mains voltage. C_F needs to be quite a big capacitor (in the uF) to have small residual ripple superimposed on the DC level; as a rule-of-thumb, use a time constant $R_L \cdot C_F$ at least 4-5 times the maximum line cycle period in case of half-wave sensing, 2-3 times in case of full-wave sensing. Then fine tune if needed, considering also transient conditions such as mains missing cycles. Brownout level does not depend on the load. When the input source is removed, C_F is discharged after some ten ms then this circuit is suitable for a quick restart after a latched shutdown.

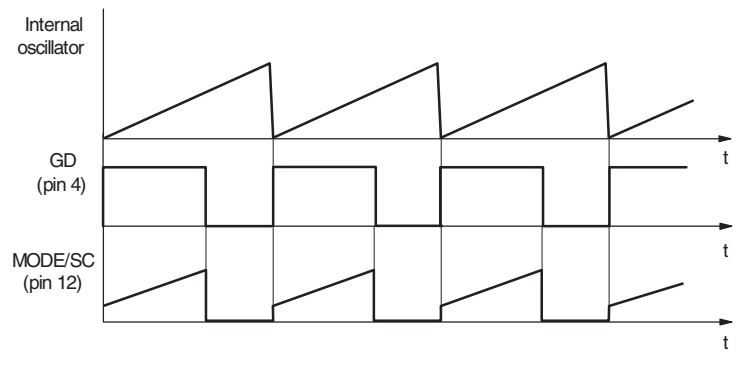
The AC_OK pin is a high impedance input connected to high value resistors, therefore it is prone to pick-up noise, which might alter the OFF threshold when the converter is running or lead to undesired switch-off of the device during ESD tests. It is possible to bypass the pin to ground with a small film capacitor (e.g. 1-10 nF) to prevent any malfunctioning of this kind.

The voltage on the pin is clamped upwards at about 3.15 V; then, if the function is not used, the pin must be connected to Vcc through a resistor (220 to 680 kΩ).

5.13 Slope compensation

The MODE/SC pin (12), when not connected to VREF, provides a voltage ramp during MOSFET ON-time synchronous to that of the internal oscillator sawtooth, with 0.8 mA minimum current capability. This ramp is intended for implementing additional slope compensation on current sense. This is needed to avoid the sub-harmonic oscillation that arises in all peak-current-mode-controlled converters working at fixed frequency in continuous conduction mode with a duty cycle close to or exceeding 50%.

Figure 27. Slope compensation waveforms



The compensation is realized by connecting a programming resistor between this pin and the current sense input (pin 7, CS). The CS pin must be connected to the sense resistor with another resistor to make a summing node on the pin. Since no ramp is delivered during MOSFET OFF-time (see *Figure 27*), no external component other than the programming resistor is needed to ensure a clean operation at light loads.

Note: The addition of the slope compensation ramp reduces the available dynamics of the current signal; thereby, the value of the sense resistor must be determined taking this into account. Note also that the burst-mode threshold (in terms of power) is slightly changed.

If slope compensation is not required with FF operation, the pin is left floating.

5.14 Summary of L6566BH power management functions

The device is provided with a number of power management functions: multiple operating mode upon loading conditions and protection functions. To help the user familiarize themselves with these functions, in the following tables, all themes are summarized with their respective activation mechanism and the resulting status of the most important pins. This can be useful not only for a correct use of the IC but also for diagnostic purposes: especially at the prototyping/debugging stage, it is quite common to come across unwanted activation of some function, and these tables can be used as a kind of quick troubleshooting guide.

Table 5. L6566BH light load management features

Feature	Description	Caused by	IC behavior	V_{CC}_restart (V)	Consump. (Iqdis,mA)	VREF (V)	SS	VCOMP (V)	OSC (V)	FMOD
Burst mode	Controlled ON-OFF operation for low power consumption at light load	$V_{COMP} < V_{COMPBM - Hys}$	Pulse skipping operation	N.A.	1.34 mA	5	Unchanged	$V_{COMPBM-HYS}$ to V_{COMPBM}	0/1	0

Table 6. L6566BH protection

Protection	Description	Caused by	IC behavior	Vcc restart (V)	IC Iq (mA)	VREF (V)	SS	VCOMP (V)	OSC (V)	FMOD	VFF
OVP	Output overvoltage protection	$V_{ZCD}>V_{ZCDth}$ for 4 consecutive switching cycles	Auto restart(1)	5	2.2	5(6)	Unchanged (6)	0	0	0	Unchanged
		VFF > VFFlatch	Latched	13.5	0.33	0	0	0	0	0	0
OLP	Output overload protection	$V_{COMP} = V_{COMPHi}$ $V_{SS} > V_{SSDIS}$	Auto restart(2)	5	1.46	5(6)	$V_{SS} < V_{SSLAT}$(3)	V_{COMPHi} (6)	0	0	Unchanged
		$V_{COMP} = V_{COMPHi}$ $V_{SS} > V_{SSLAT}$	Latched	13.5	0.33	0	0	0	0	0	0
Short-circuit protection	Output short-circuit protection	$V_{COMP} = V_{COMPHi}$ $V_{SS} > V_{SSDIS}$(4)	Auto restart	5	1.46	0	$V_{SS} < V_{SSLAT}$(6)	V_{COMPHi}(5)		0	Unchanged
		$V_{COMP} = V_{COMPHi}$ $V_{SS} > V_{SSLAT}$(6)	Latched	13.5	0.33	0	0	0	0	0	0
2nd OCP	Transformer saturation or shorted secondary diode protection	$V_{CS} > V_{CSDIS}$ for 2-3 consecutive switching cycles	Latched	5	0.33	0	0	0	0	0	0

Table 6. L6566BH protection (continued)

Protection	Description	Caused by	IC behavior	Vcc restart (V)	IC Iq (mA)	VREF (V)	SS	VCOMP (V)	OSC (V)	FMOD	VFF
OTP	Externally settable overtemperature protection	$V_{DIS}>V_{OTP}$	Latched	13.5	0.33	0	0	0	0	0	0
	Internal shutdown	$T_j > 160\ ^oC$	Auto restart(5)	5	0.33	0	0	0	0	0	0
Brownout	Mains undervoltage protection	$V_{AC_OK} < V_{th}$	Auto restart	5	0.33	0	0	0	0	0	Unchanged
Reference drift	V_{REF} drift protection	$V_{REF} > V_{ov}$	Latched	13.5	0.33	0	0	0	0	0	0
Shutdown1	Gate driver disable	$V_{FF} > V_{off}$	Auto restart	5	2.5	5	Unchanged	Unchanged	1	Unchanged	Unchanged
Shutdown2	Shutdown by V_{COMP} low	$V_{COMP} < V_{COMPOFF}$	Latched	10	0.33	0	0	0	0	0	0
Adaptive UVLO	Shutdown by V_{cc} going below V_{ccoff} (lowering of V_{ccoff} threshold at light load)	$V_{cc} < 9.4$ V ($V_{COMP} > V_{COMPL}$)	Auto restart	5 V	0.18mA	0	0	0	0	0	0
		$V_{cc} < 7.2$ V ($V_{COMP} > V_{COMPO}$)									

1. Use one external diode from V_{FF} (#15) to AC_OK (#16), cathode to AC_OK.
2. Use one external diode from SS (#14) to V_{REF} (#10), cathode to V_{REF}.
3. If C_{ss} and the V_{cc} capacitor are such that V_{cc} falls below UVLO before latch tripping (*Figure 21*).
4. If C_{ss} and the Vcc capacitor are such that the latch is tripped before V_{cc} falls below UVLO (*Figure 21*).
5. When $T_J < 110\ ^oC$.
6. Discharged to zero by V_{cc} going below UVLO.

It is worth remembering that “auto-restart” means that the device works intermittently as long as the condition that is activating the function is not removed; “Latched” means that the device is stopped as long as the unit is connected to the input power source and the unit must be disconnected for some time from the source in order for the device (and the unit) to restart. Optionally, a restart can be forced by pulling the voltage of pin 16 (AC_OK) below 0.45 V.

6 Application examples and ideas

Figure 28. Typical low-cost application schematic

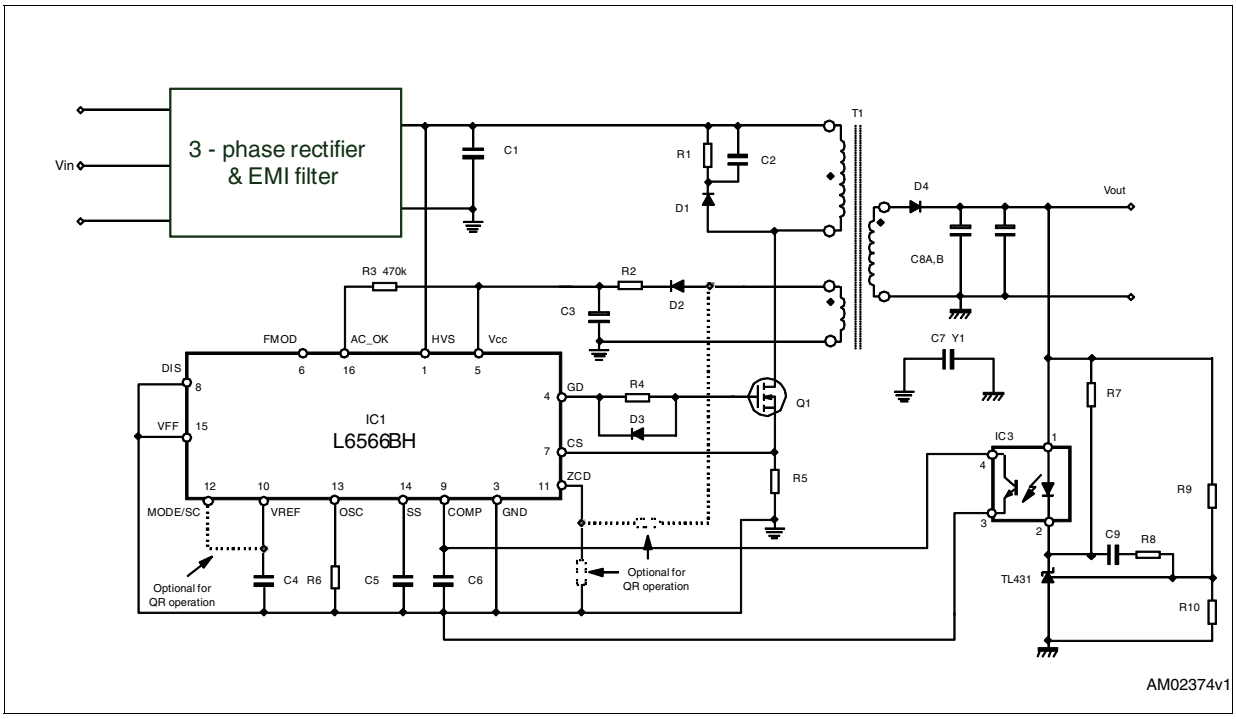


Figure 29. Typical full-feature application schematic (QR operation)

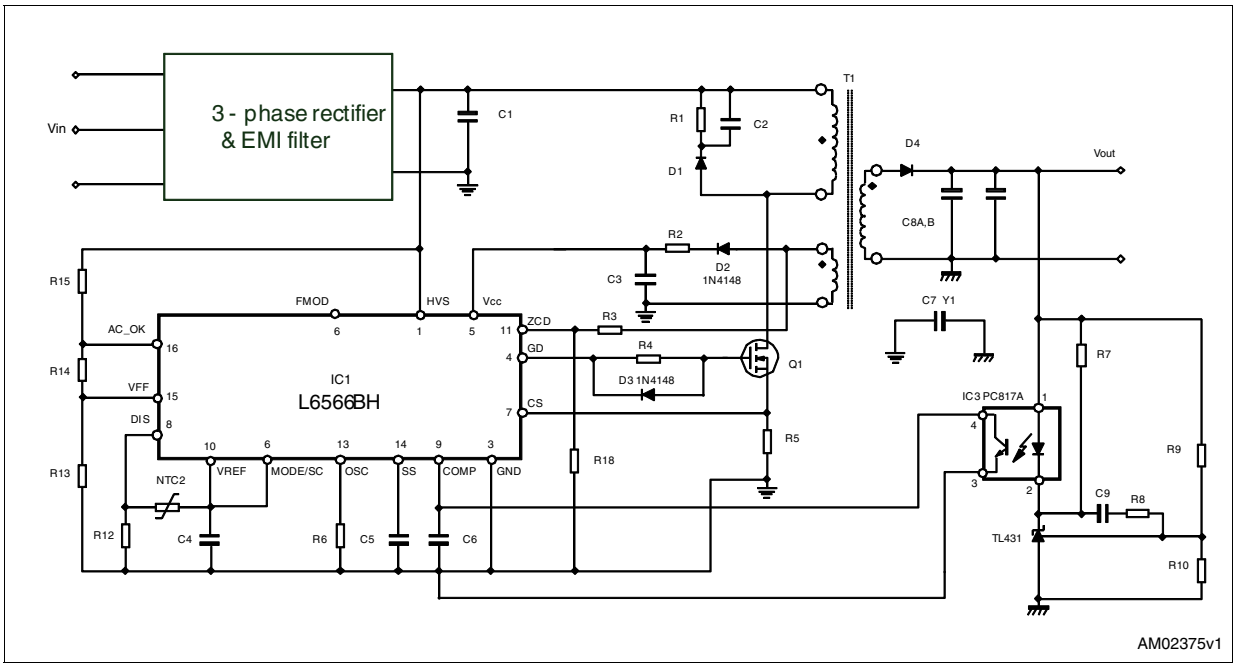


Figure 30. Typical full-feature application schematic (FF operation)

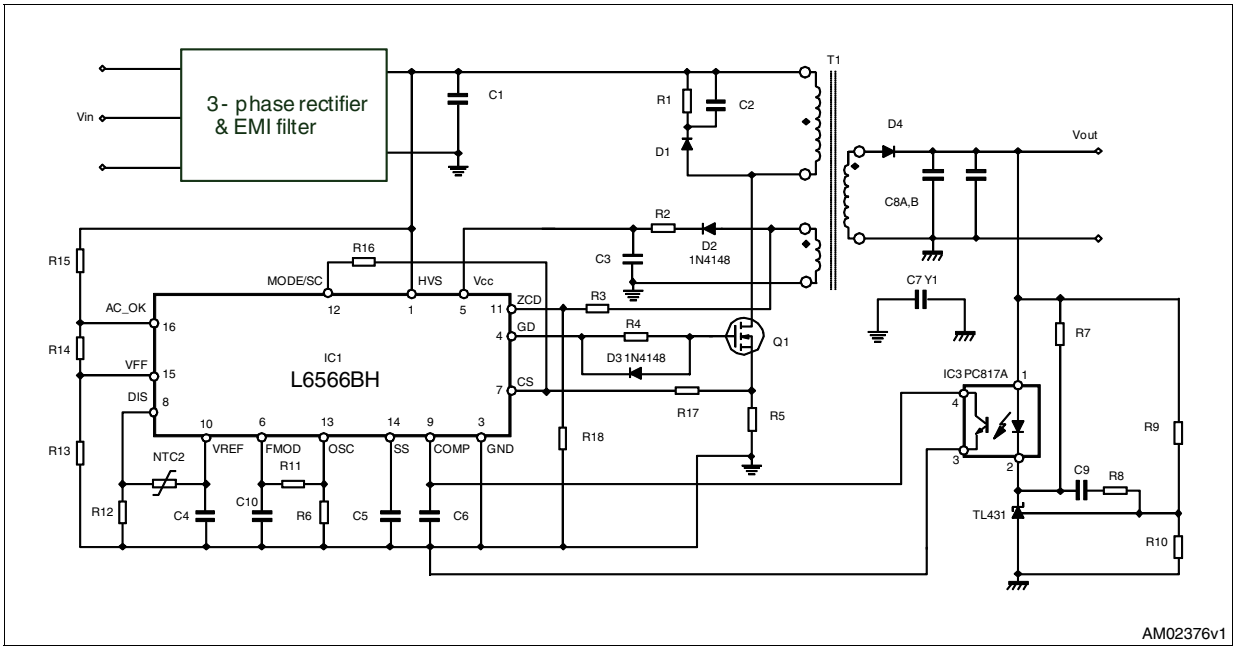


Table 7. External circuits that determine IC behavior upon OVP and OCP

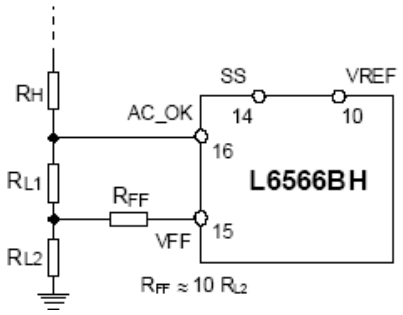
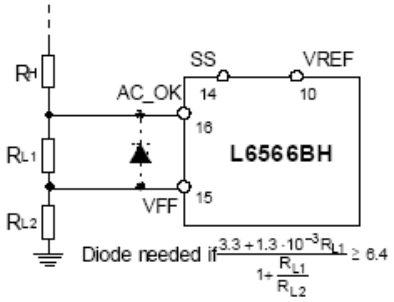
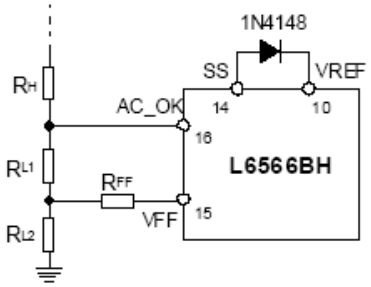
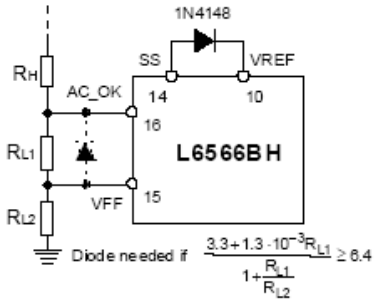
	OVP latched	OVP auto-restart
OCP latched		
OCP auto-restart		

Figure 31. Frequency foldback at light load (FF operation)

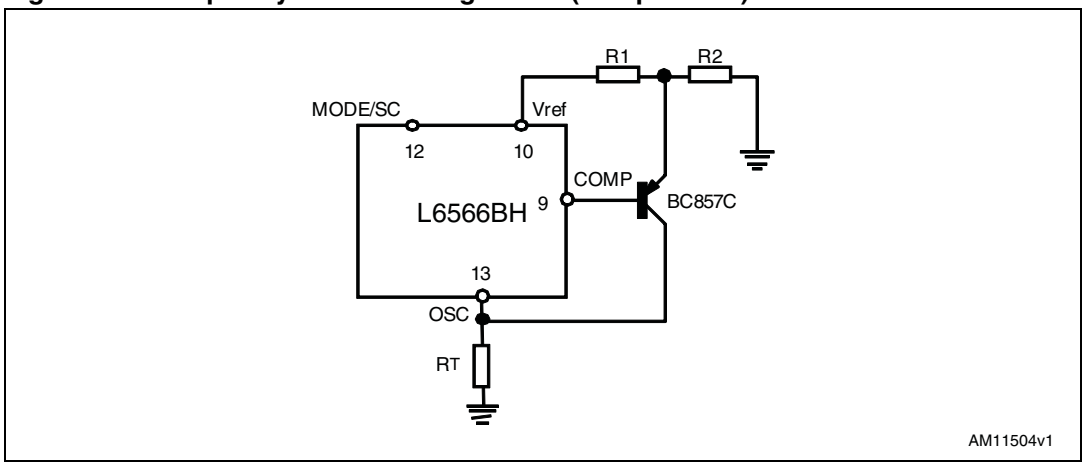
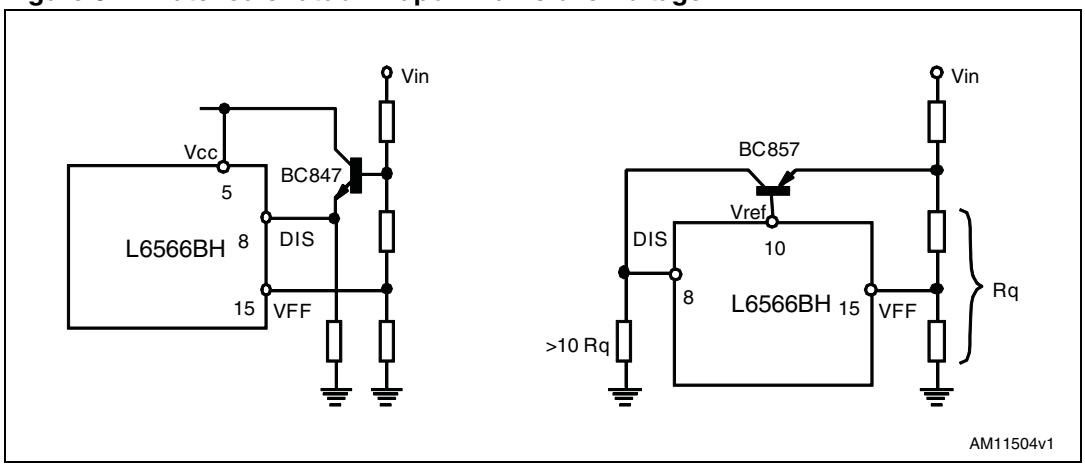


Figure 32. Latched shutdown upon mains overvoltage



7 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 8. SO16N mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.31		0.51
c	0.17		0.25
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
k	0		8°
ccc			0.10

Figure 33. SO16N package drawing

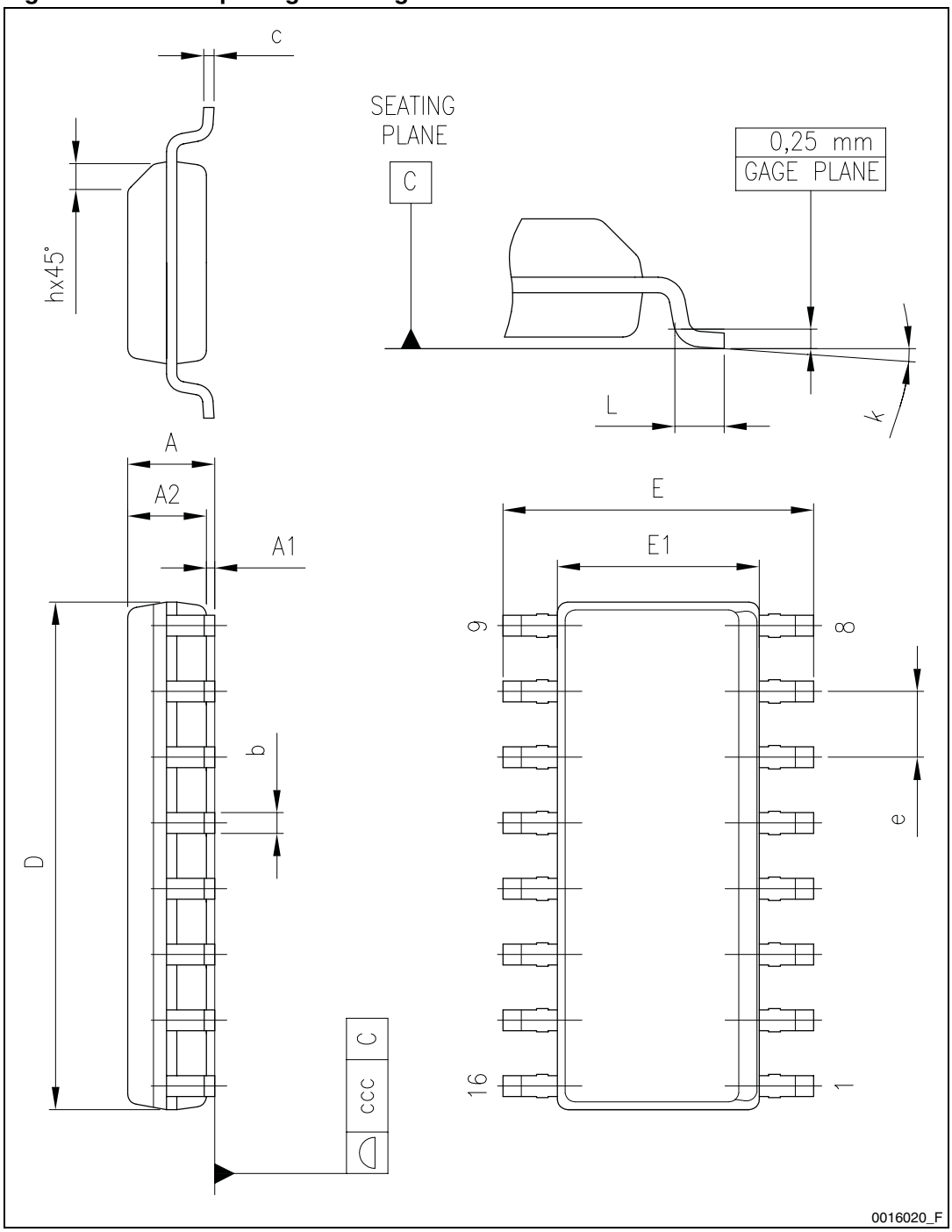
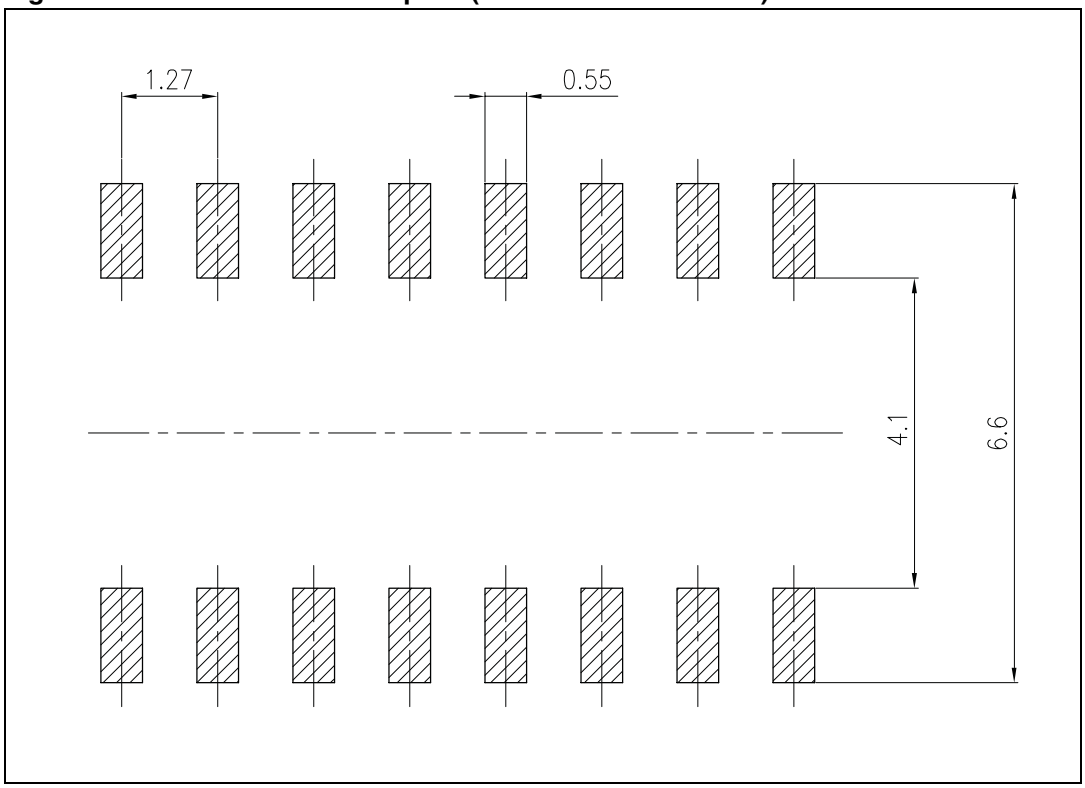


Figure 34. Recommended footprint (dimensions are in mm)



8 Order codes

Table 9. Order codes

Order codes	Package	Packaging
L6566BH	SO16N	Tube
L6566BHTR	SO16N	Tape and reel

9 Revision history

Table 10. Document revision history

Date	Revision	Changes
30-Nov-2009	1	First release
16-Apr-2012	2	Updated internal voltage reference: typical value from 800 V to 840 V in the entire document. Updated: *Table 2* and *Table 4*. Added footnote 4 on *Table 4*. Updated *Figure 8*. and *Section 7: Package mechanical data*. Minor text changes.

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