EVALUATION KIT AVAILABLE

MAX17595/MAX17596/MAX17597

Peak-Current-Mode Controllers for Flyback and Boost Regulators

General Description

The MAX17595/MAX17596/MAX17597 is a family of peak-current-mode controllers which contain all the circuitry required for the design of wide input-voltage flyback and boost regulators. The MAX17595 offers optimized input rising and falling thresholds for universal input AC-DC converters and telecom DC-DC (36V–72V input range) power supplies. The MAX17596 offers input rising and falling thresholds suitable for low-voltage DC-DC applications (4.5V–36V input range). The MAX17597 offers all circuitry needed to implement a boost converter controller. All three controllers contain a built-in gate driver for external n-channel MOSFETs.

The MAX17595/MAX17596/MAX17597 house an internal error amplifier with 1% accurate reference, useful in implementations without the need for an external reference. The switching frequency is programmable from 100kHz to 1MHz with an accuracy of 8% using an external resistor, allowing optimization of magnetic and filter components, resulting in compact and cost-effective power conversion solutions. For EMI sensitive applications, the MAX17595/MAX17596/MAX17597 family incorporates a programmable-frequency dithering scheme, enabling low-EMI spread-spectrum operation.

An EN/UVLO input allows the user to start the power supply precisely at the desired input voltage, while also functioning as an on/off pin. The OVI pin enables implementation of an input overvoltage protection scheme, ensuring that the converter shuts down when the DC input voltage exceeds a set maximum value. The SS pin allows programmable soft-start time for the power converter, and helps limit inrush current during startup. The MAX17595/MAX17596/MAX17597 family also allows the designer to choose between voltage soft-start and current soft-start modes, useful in optoisolated designs. A programmable slope compensation scheme is provided to enhance the stability of the peak-current-mode control scheme.

Hiccup-mode overcurrent protection and thermal shutdown are provided to minimize dissipation in overcurrent and overtemperature fault conditions. The IC is available in a space-saving 16-pin, 3mm x 3mm TQFN package with 0.5mm lead spacing.

Benefits and Features

- **Peak Current Mode Offline (Universal Input AC) and Telecom (36V–72V) Flyback Controller (MAX17595)**
- **Peak-Current-Mode DC-DC Flyback Controller (4.5V–36V Input Range) (MAX17596)**
- **Peak-Current-Mode Nonsynchronous Boost PWM Controller (4.5V–36V Input Range) (MAX17597)**
- **Current Mode Control Provides Excellent Transient Response**
- **Low 20µA Startup Supply Current**
- **100kHz to 1MHz Programmable Switching Frequency**
- **Programmable Frequency Dithering for Low-EMI Spread-Spectrum Operation**
- **Switching Frequency Synchronization**
- **Adjustable Current Limit with External Current-Sense Resistor**
- **Fast Cycle-By-Cycle Peak Current Limiting**
- **Hiccup-Mode Short-Circuit Protection**
- **Overtemperature Protection**
- **Programmable Soft-Start and Slope Compensation**
- **Programmable Voltage or Current Soft-Start Schemes**
- **Input Overvoltage Protection**
- **Space-Saving, 3mm x 3mm TQFN Package**

Applications

Universal Input Offline AC-DC Power Supplies

Wide-Range DC-Input Flyback/Boost Battery Chargers

Battery-Powered Applications

Industrial, Telecom, and Automotive Applications

***Ordering Information/Selector Guide* appears at end of data sheet.**

*For related parts and recommended products to use with this part, refer to **www.maxim-ic.com/MAX17595.related**.*

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maximintegrated.com.

19-6178; Rev 0; 1/12

ABSOLUTE MAXIMUM RATINGS

V_{IN} to SGND ..... -0.3V to +40V
V_{DRV} to SGND ..... -0.3V to +16V (MAX17595)
V_{DRV} to SGND ..... -0.3V to +6V (MAX17596 and MAX17597)
NDRV to SGND ..... -0.3V to +(V_{DRV} + 0.3)V
EN/UVLO to SGND ..... -0.3V to +(V_{IN} + 0.3)V
OVI, RT, DITHER, COMP, SS, FB, SLOPE to SGND ..... -0.3V to +6V
CS to SGND ..... -0.8V to +6V
PGND to SGND ..... -0.3V to +0.3V

Maximum Input/Output Current (Continuous)
V_{IN}, NDRV 100mA
NDRV (pulsed, for less than 100ns) ..... ±1A
Continuous Power Dissipation TQFN (single-layer board) (derate 20.8mW/°C above +70°C) 1666mW
Operating Temperature Range ..... -40°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... 48°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) ..... 7°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 12V (for the MAX17595, bring V_{IN} up to 21V for startup), V_{CS} = V_{SLOPE} = V_{DITHER} = V_{FB} = V_{OVI} = V_{SGND} = 0V, $V_{EN/UVLO}$ = +2V; NDRV, SS, COMP are unconnected, R_{RT} = 25kΩ, C_{VIN} = 1µF, C_{VDRV} = 1µF, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = T_J = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
INPUT SUPPLY (V_{IN})							
V_{IN} Voltage Range	V_{IN}	MAX17595		8		29	V
		MAX17596/MAX17597		4.5		36	
V_{IN} Bootstrap UVLO Wakeup	V_{IN-UVR}	V_{IN} rising ↑	MAX17595	18.5	20	21.5	V
			MAX17596/MAX17597	3.5	4	4.4	
V_{IN} Bootstrap UVLO Shutdown Level	V_{IN-UVF}	V_{IN} falling ↓	MAX17595	6.5	7	7.7	V
			MAX17596/MAX17597	3.3	3.9	4.25	
V_{IN} Supply Start-Up Current (Under UVLO)	$I_{VIN-STARTUP}$	V_{IN} < UVLO			20	32	µA
V_{IN} Supply Shutdown Current	I_{IN-SH}	V_{EN} = 0V			20	32	µA
V_{IN} Supply Current	I_{IN-SW}	Switching, f_{SW} = 400kHz			2		mA
V_{IN} CLAMP (INC) (MAX17595 ONLY)							
V_{IN} Clamp Voltage	V_{INC}	MAX17595, I_{VIN} = 2mA sinking, V_{EN} = 0V (Note 3)		30	33	36	V
ENABLE (EN)							
EN Undervoltage Threshold	V_{ENR}	V_{EN} rising ↑		1.16	1.21	1.26	V
	V_{ENF}	V_{EN} falling ↓		1.1	1.15	1.2	
EN Input Leakage Current	I_{EN}	V_{EN} = 1.5V, T_A = +25°C		-100		+100	nA

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 12V (for the MAX17595, bring V_{IN} up to 21V for startup), V_{CS} = V_{SLOPE} = V_{DITHER} = V_{FB} = V_{OVI} = V_{SGND} = 0V, $V_{EN/UVLO}$ = +2V; NDRV, SS, COMP are unconnected, R_{RT} = 25kΩ, C_{VIN} = 1µF, C_{VDRV} = 1µF, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = T_J = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INTERNAL LDO (VDRV)						
V_{DRV} Output Voltage Range	V_{DRV}	8V < V_{IN} < 15V and 0mA < I_{VDRV} < 50mA (MAX17595)	7.1	7.4	7.7	V
		6V < V_{IN} < 12V and 0mA < I_{VDRV} < 50mA (MAX17596/MAX17597)	4.7	4.9	5.1	
V_{DRV} Current Limit	$I_{VDRV-MAX}$		70	100		mA
V_{DRV} Dropout	$V_{VDRV-DO}$	V_{IN} = 4.5V, I_{VDRV} = 20mA (MAX17596/MAX17597)	4.2			V
OVERVOLTAGE PROTECTION (OVI)						
OVI Overvoltage Threshold	V_{OVIR}	V_{OVI} rising ↑	1.16	1.21	1.26	V
	V_{OVIF}	V_{OVI} falling ↓	1.1	1.15	1.2	
OVI Masking Delay	t_{OVI-MD}			2		µs
OVI Input Leakage Current	I_{OVI}	V_{OVI} = 1V, T_A = +25°C	-100		+100	nA
OSCILLATOR (RT)						
NDRV Switching Frequency Range	f_{SW}		100		1000	kHz
NDRV Switching Frequency Accuracy			-8		+8	%
Maximum Duty Cycle	D_{MAX}	(MAX17595/MAX17596)	46	48	50	%
		(MAX17597)	90	92.5	95	
SYNCHRONIZATION (DITHER)						
Synchronization Logic-High Input	$V_{HI-SYNC}$		3			V
Synchronization Pulse Width				50		ns
Synchronization Frequency Range	f_{SYNCIN}	(MAX17595/MAX17596)	1.1 x f_{SW}		1.8 x f_{SW}	Hz
DITHERING RAMP GENERATOR (DITHER)						
Charging Current		V_{DITHER} = 0V	45	50	55	µA
Discharging Current		V_{DITHER} = 2.2V	43	50	57	µA
Ramp-High Trip Point				2		V
Ramp-Low Trip Point				0.4		V

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 12V (for the MAX17595, bring V_{IN} up to 21V for startup), V_{CS} = V_{SLOPE} = V_{DITHER} = V_{FB} = V_{OVI} = V_{SGND} = 0V, $V_{EN/UVLO}$ = +2V; NDRV, SS, COMP are unconnected, R_{RT} = 25kΩ, C_{VIN} = 1µF, C_{VDRV} = 1µF, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = T_J = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SOFT-START/SOFT-STOP (SS)						
Soft-Start Charging Current	I_{SSCH}		9	10	11	µA
Soft-Stop Discharging Current	$I_{SSDISCH}$	For soft-stop enabled parts	4.4	5	5.6	µA
SS Bias Voltage	V_{SS}		1.19	1.21	1.23	V
SS Discharge Threshold	$V_{SSDISCH}$	Soft-stop completion		0.15		V
NDRV DRIVER (NDRV)						
Pulldown Impedance	R_{NDRV-N}	I_{NDRV} (sinking) = 100mA		1.37	3	Ω
Pullup Impedance	R_{NDRV-P}	I_{NDRV} (sourcing) = 5mA		4.26	8.5	Ω
Peak Sink Current		C_{NDRV} = 10nF		1.5		A
Peak Source Current		C_{NDRV} = 10nF		0.9		A
Fall Time	t_{NDRV-F}	C_{NDRV} = 1nF		10		ns
Rise Time	t_{NDRV-R}	C_{NDRV} = 1nF		20		ns
CURRENT-LIMIT COMPARATOR (CS)						
Cycle-by-Cycle Peak -Current-Limit Threshold	$V_{CS-PEAK}$		290	305	320	mV
Cycle-by-Cycle Runaway Current-Limit Threshold	V_{CS-RUN}		340	360	380	mV
Cycle-by-Cycle Reverse-Current Limit Threshold	V_{CS-REV}		-122	-102	-82	mV
Current-Sense Leading-Edge Blanking Time	$t_{CS-BLANK}$	From NDRV rising ↑ edge		70		ns
Propagation Delay from Comparator Input to NDRV	t_{PDCS}	From CS rising (10mV overdrive) to NDRV falling (excluding leading edge blanking)		40		ns
Number of Consecutive Peak-Current-Limit Events to Hiccup	$N_{HICCUP-P}$			8		event
Number of Runaway-Current-Limit Events to Hiccup	$N_{HICCUP-R}$			1		event
Overcurrent Hiccup Timeout				32768		cycle
Minimum On-Time	t_{ON-MIN}		90	130	170	ns
SLOPE COMPENSATION (SLOPE)						
Slope Bias Current	I_{SLOPE}		9	10	11	µA
Slope Resistor Range			25		200	kΩ
Slope Voltage Range to Enable Current Soft-Start and Minimum Slope Compensation			0		200	mV

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 12V (for the MAX17595, bring V_{IN} up to 21V for startup), V_{CS} = V_{SLOPE} = V_{DITHER} = V_{FB} = V_{OVI} = V_{SGND} = 0V, $V_{EN/UVLO}$ = +2V; NDRV, SS, COMP are unconnected, R_{RT} = 25kΩ, C_{VIN} = 1µF, C_{VDRV} = 1µF, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = T_J = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Slope Voltage Range to Enable Voltage Soft-Start and Minimum Slope Compensation			4			V
Slope Voltage Range to Enable Voltage Soft-Start and Programmable Slope Compensation			0.2		4	V
Slope Compensation Ramp		R_{SLOPE} = 100kΩ	140	165	190	mV/µs
Default Slope Compensation Ramp		V_{SLOPE} < 0.2V or 4V < V_{SLOPE}		50		mV/µs
PWM COMPARATOR						
Comparator Offset Voltage	V_{PWM-OS}	V_{COMP} - V_{CS}	1.65	1.81	2	V
Current-Sense Gain	A_{CS-PWM}	ΔCOMP/ΔCS (T_A = +25°C)	1.75	1.97	2.15	V/V
CS Peak Slope Ramp Current	$I_{CSSLOPE}$	Ramp current peak (T_A = +25°C)		13	20	µA
Comparator Propagation Delay	t_{PWM}	Change in V_{CS} = 10mV (including internal lead-edge blanking)		110		ns
ERROR AMPLIFIER						
FB Reference Voltage	V_{REF}	V_{FB}, when I_{COMP} = 0 and V_{COMP} = 1.8V	1.19	1.21	1.23	V
FB Input Bias Current	I_{FB}	V_{FB} = 1.5V, T_A = +25°C	-100		+100	nA
Voltage Gain	A_{EAMP}			80		dB
Transconductance	Gm		1.5	1.8	2.1	mS
Transconductance Bandwidth	BW	Open-loop (gain = 1), -3dB frequency		10		MHz
Source Current		V_{COMP} = 1.8V, V_{FB} = 1V	80	120	210	µA
Sink Current		V_{COMP} = 1.8V, V_{FB} = 1.75V	80	120	210	µA
THERMAL SHUTDOWN						
Thermal Shutdown Threshold		Temperature rising		+160		°C
Thermal Shutdown Hysteresis				20		°C

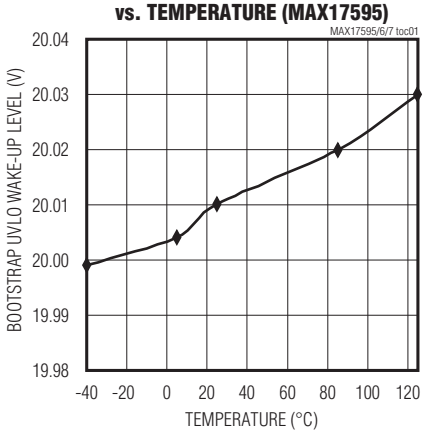
Note 2: All devices 100% production tested at T_A = +25°C. Limits over temperature are guaranteed by design.

Note 3: The MAX17595 is intended for use in universal input power supplies. The internal clamp circuit at V_{IN} is used to prevent the bootstrap capacitor from changing to a voltage beyond the absolute maximum rating of the device when EN is low (shutdown mode). Externally limit the maximum current to V_{IN} (hence to clamp) to 2mA (max) when EN is low.

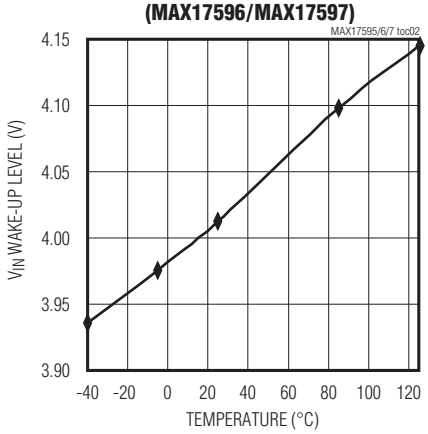
Typical Operating Characteristics

(V_{IN} = 15V, $V_{EN/UVLO}$ = +2V, COMP = open, C_{VIN} = 1µF, C_{VCC} = 1µF, T_A = T_J = -40°C to +125°C, unless otherwise noted.)

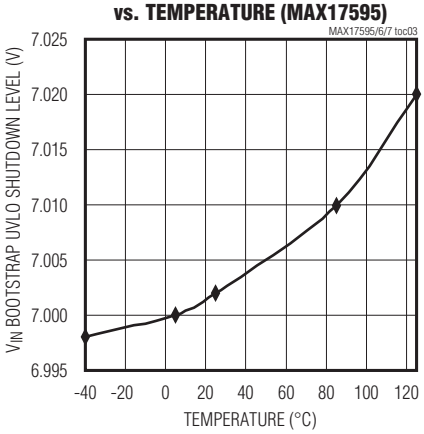
BOOTSTRAP UVLO WAKE-UP LEVEL vs. TEMPERATURE (MAX17595)



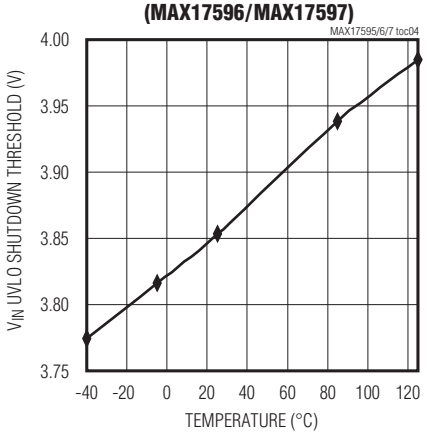
V_{IN} WAKE-UP LEVEL vs. TEMPERATURE (MAX17596/MAX17597)



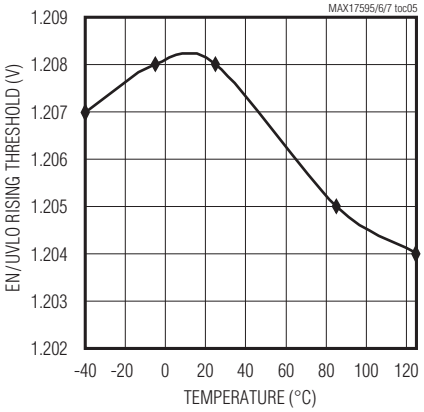
V_{IN} FALLING THRESHOLD vs. TEMPERATURE (MAX17595)



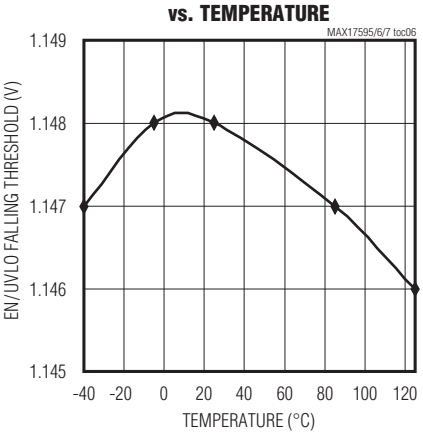
V_{IN} FALLING THRESHOLD vs. TEMPERATURE (MAX17596/MAX17597)



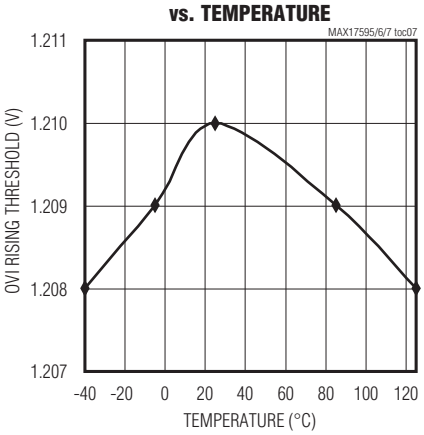
EN/UVLO RISING THRESHOLD vs. TEMPERATURE



EN/UVLO FALLING THRESHOLD vs. TEMPERATURE



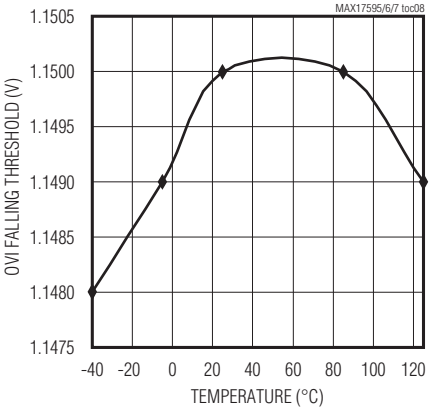
OVI RISING THRESHOLD vs. TEMPERATURE



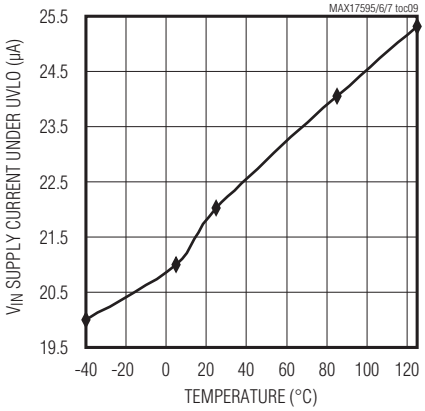
Typical Operating Characteristics (continued)

(V_{IN} = 15V, $V_{EN/UVLO}$ = +2V, COMP = open, C_{VIN} = 1µF, C_{VCC} = 1µF, T_A = T_J = -40°C to +125°C, unless otherwise noted.)

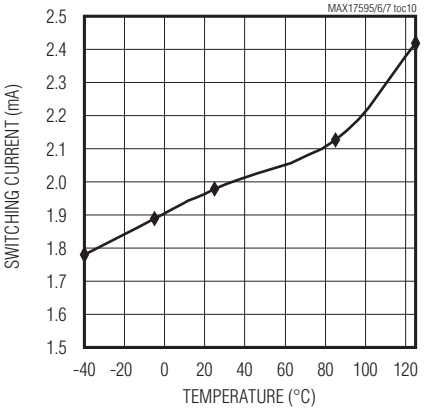
OVI FALLING THRESHOLD vs. TEMPERATURE



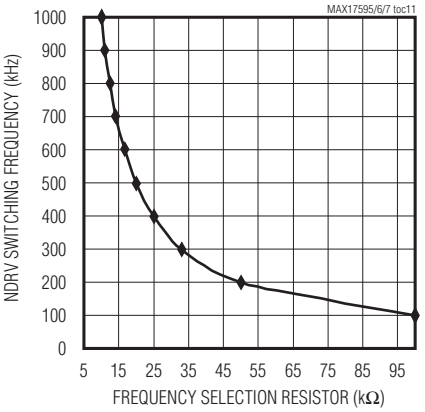
V_{IN} SUPPLY CURRENT UNDER UVLO vs. TEMPERATURE



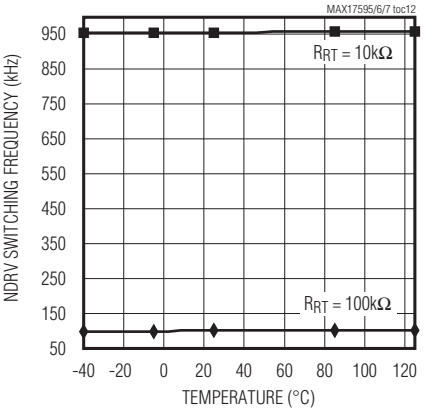
SWITCHING CURRENT vs. TEMPERATURE



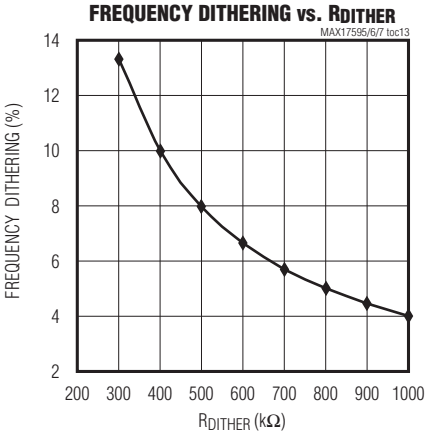
NDRV SWITCHING FREQUENCY vs. RESISTOR



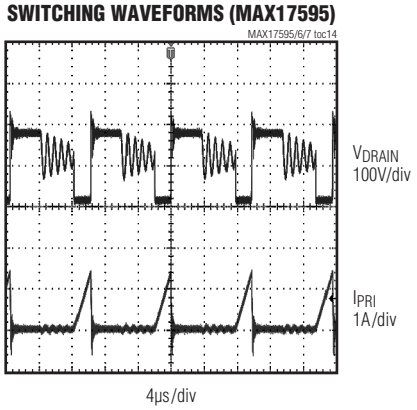
NDRV SWITCHING FREQUENCY vs. TEMPERATURE



FREQUENCY DITHERING vs. R_{DITHER}



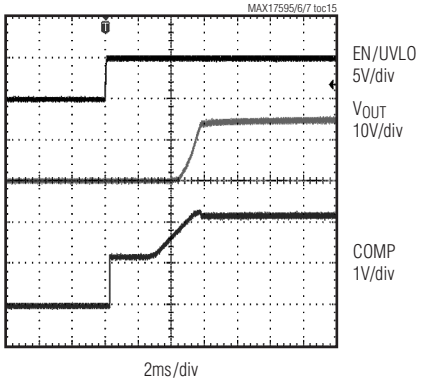
SWITCHING WAVEFORMS (MAX17595)



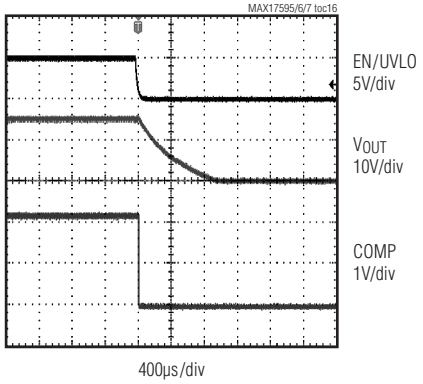
Typical Operating Characteristics (continued)

(V_{IN} = 15V, $V_{EN/UVLO}$ = +2V, COMP = open, C_{VIN} = 1µF, C_{VCC} = 1µF, T_A = T_J = -40°C to +125°C, unless otherwise noted.)

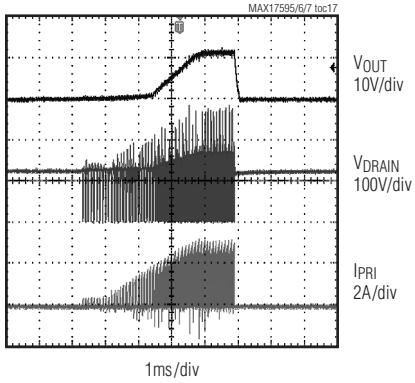
ENABLE STARTUP



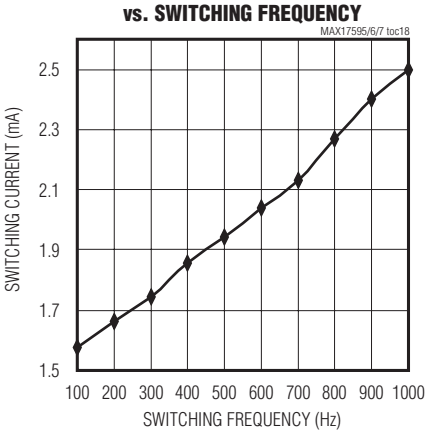
ENABLE SHUTDOWN



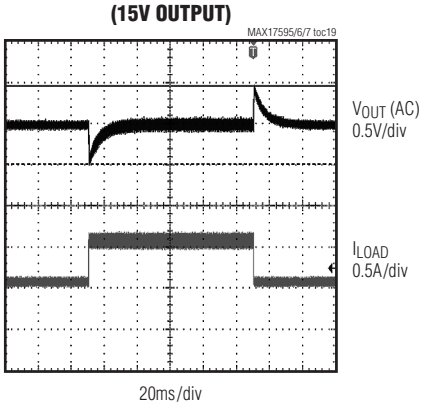
HICCUP OPERATION



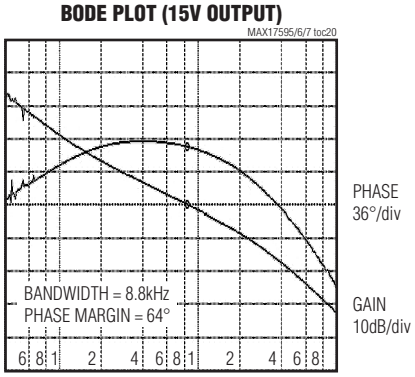
SWITCHING CURRENT vs. SWITCHING FREQUENCY



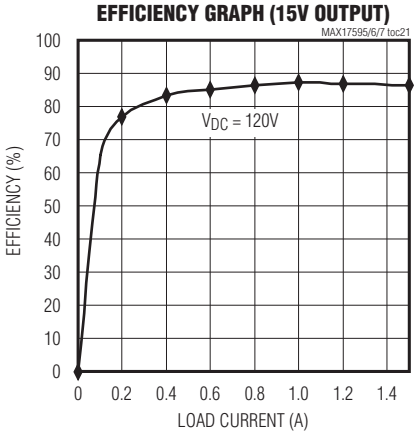
LOAD TRANSIENT RESPONSE (15V OUTPUT)



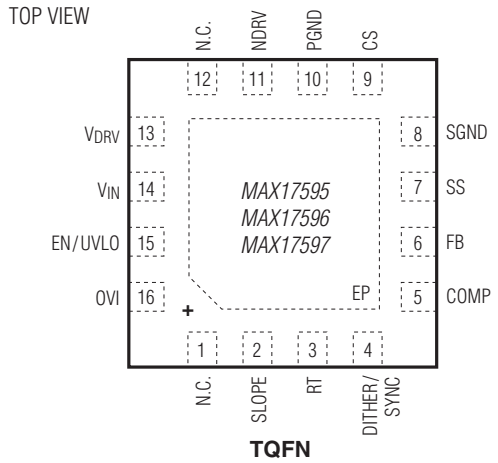
BODE PLOT (15V OUTPUT)



EFFICIENCY GRAPH (15V OUTPUT)



Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1, 12	N.C.	No Connection
2	SLOPE	Slope Compensation Input. A resistor, R_{SLOPE}, connected from SLOPE to SGND programs the amount of slope compensation with reference-voltage soft-start mode. Connecting this pin to SGND enables duty-cycle soft-start with minimum slope compensation of 50mV/µs. Setting V_{SLOPE} > 4V enables reference voltage soft-start with minimum slope compensation of 50mV/µs.
3	RT	Switching Frequency Programming Resistor Connection. Connect resistor R_{RT} from RT to SGND to set the PWM switching frequency.
4	DITHER/SYNC	Frequency Dithering Programming or Synchronization Connection. For spread-spectrum frequency operation, connect a capacitor from DITHER to SGND, and a resistor from DITHER to RT. To synchronize the internal oscillator to the externally applied frequency, connect DITHER/SYNC to the synchronization pulse.
5	COMP	Transconductance Amplifier Output. Connect the frequency compensation network between COMP and SGND.
6	FB	Transconductance Amplifier Inverting Input
7	SS	Soft-Start Capacitor Pin for Flyback Regulator. Connect a capacitor C_{SS} from SS to SGND to set the soft-start time interval.
8	SGND	Signal Ground. Connect SGND to the signal ground plane.
9	CS	Current-Sense Input. Peak-current-limit trip voltage is 300mV.
10	PGND	Power Ground. Connect PGND to the power ground plane.
11	NDRV	External Switching nMOS Gate-Driver Output

Pin Description (continued)

PIN	NAME	FUNCTION
13	V_{DRV}	Linear Regulator Output and Driver Input. Connect input bypass capacitor from V_{DRV} to SGND as close as possible to the IC.
14	V_{IN}	Internal V_{DRV} Regulator Input. Connect V_{IN} to the input voltage source. Bypass V_{IN} to PGND with a 1µF minimum ceramic capacitor.
15	EN/UVLO	Enable/Undervoltage Lockout. To externally program the UVLO threshold of the input supply, connect a resistive divider between input supply, EN, and SGND.
16	OVI	Overvoltage Comparator Input. Connect a resistive divider between the input supply, OVI, and SGND to set the input overvoltage threshold.
—	EP	Exposed Pad

Detailed Description

The MAX17595 offers a bootstrap UVLO wakeup level of 20V with a wide hysteresis of 15V minimum, and is optimized for implementing isolated and non-isolated universal (85V to 265V AC) offline single-switch flyback converter or telecom (36V to 72V) power supplies. The MAX17596/MAX17597 offer a UVLO wakeup level of 4.4V and are well-suited for low-voltage DC-DC flyback/boost power supplies. An internal 1% reference (1.21V) can be used to regulate the output down to 1.21V in nonisolated flyback and boost applications. Additional semi-regulated outputs, if needed, can be generated by using additional secondary windings on the flyback converter transformer.

The MAX17595/MAX17596/MAX17597 family utilizes peak-current-mode control and external compensation for optimizing closed-loop performance. The devices include cycle-by-cycle peak current limit, and eight consecutive occurrences of current-limit-event trigger hiccup mode, which protects external components by halting switching for a period of 32,768 cycles. The devices also include voltage soft-start for nonisolated designs, and current soft-start for isolated designs to allow monotonic and smooth rise of the outpu voltage during startup. The voltage and current soft-start modes can be selected using the SLOPE pin. See *Figure 1* for more information.

Input Voltage Range (V_{IN})

The MAX17595 has different rising and falling undervoltage lockout (UVLO) thresholds on the V_{IN} pin than the thresholds of the MAX17596/MAX17597. The thresholds for the MAX17595 are optimized for implementing power supply startup schemes, typically used for offline AC-DC power supplies. The MAX17595 is well-suited for operation from rectified DC bus in AC-DC power-supply applications, which are typical of front-end industrial power-supply applications. As such, the MAX17595 has no limitation on maximum input voltage, as long as the external components are rated suitably and the maximum operating voltages of the MAX17595 are respected.

The MAX17595 can be successfully used in universal input (85V to 265V AC) rectified bus applications, in rectified 3-phase DC bus applications, and in telecom (36V to 72V DC) applications.

The MAX17596/MAX17597 are intended to implement flyback (isolated and nonisolated) and boost converters. The V_{IN} pin of the MAX17596/MAX17597 has a maximum operating voltage of 36V. The MAX17596/MAX17597 implement rising and falling thresholds on the V_{IN} pin that assume power-supply startup schemes typical of low-voltage DC-DC applications, down to an input voltage of 4.5V DC. Therefore, flyback/boost converters with a 4.5V to 36V supply voltage range can be implemented with the MAX17596/MAX17597.

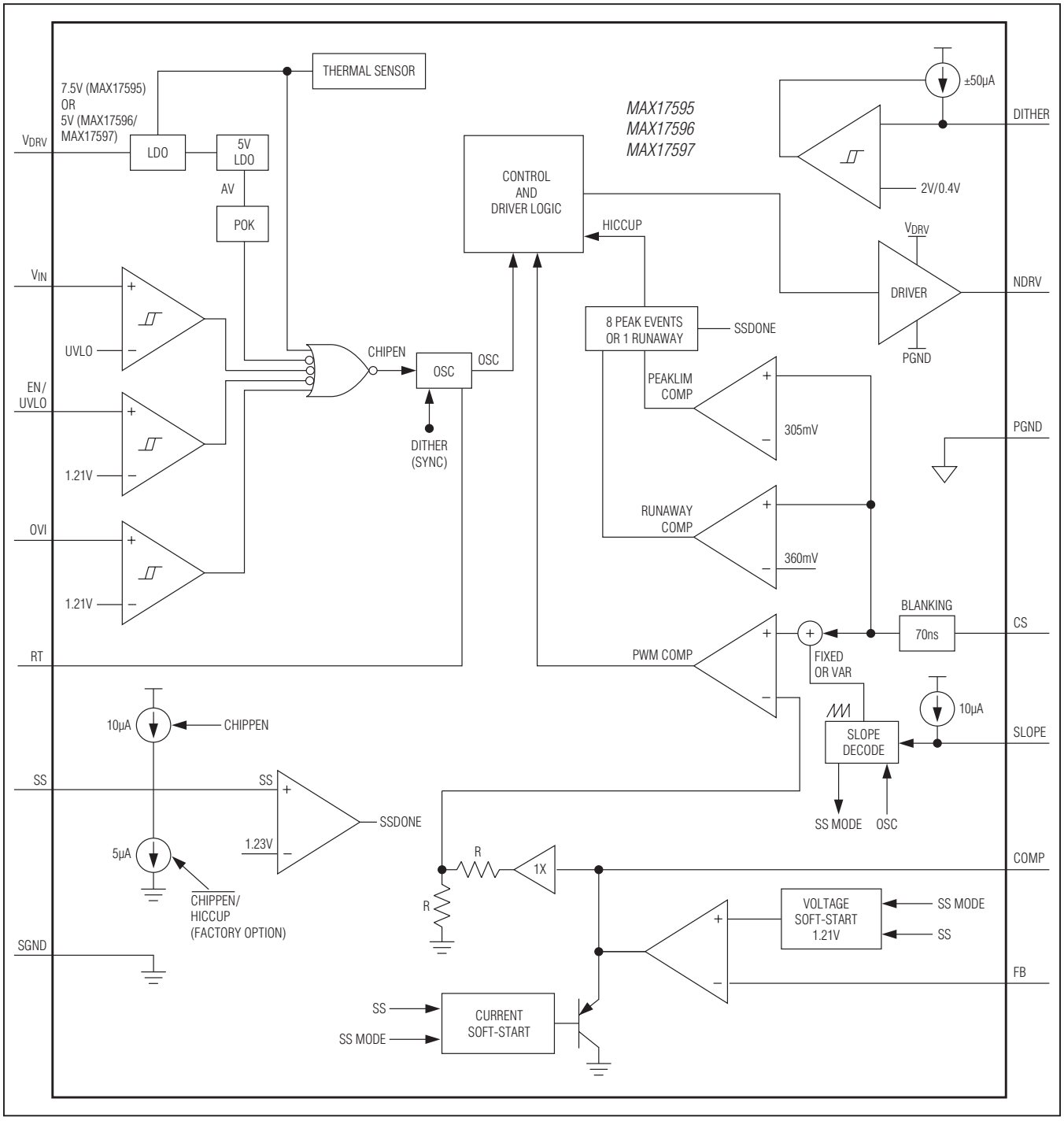


Figure 1. MAX17595/MAX17596/MAX17597 Block Diagram

Internal Linear Regulator (V_{DRV})

The internal functions and driver circuits are designed to operate from 7.5V (MAX17595) or 5V (MAX17596/MAX17597) power supply voltages. The MAX17595/MAX17596/MAX17597 family has an internal linear regulator that is powered from the V_{IN} pin. The output of the linear regulator is connected to the V_{DRV} pin, and should be decoupled with a 1µF capacitor to ground for stable operation. The V_{DRV} regulator output supplies all the operating current of the MAX17595/MAX17596/MAX17597. The maximum operating voltage on the V_{IN} pin is 29V for the MAX17595, and 36V for the MAX17596/MAX17597.

n-Channel MOSFET Gate Driver (NDRV)

The MAX17595/MAX17596/MAX17597 family offers a built-in gate driver for driving an external n-channel MOSFET. The NDRV pin can source/sink currents in excess of 650mA/1000mA.

Maximum Duty Cycle

The MAX17595/MAX17596 operate at a maximum duty cycle of 49%. The MAX17597 offers a maximum duty cycle of 94% to implement flyback and boost converters involving large input-to-output voltage ratios in DC-DC applications. Slope compensation is necessary for stable operation of peak-current-mode controlled converters such as the MAX17595/MAX17596/MAX17597 at duty cycles greater than 50%, in addition to the loop compensation required for small signal stability. The MAX17595/MAX17596/MAX17597 implement a SLOPE pin for this purpose. See the *Slope Compensation* section for more details.

Soft-Start (SS)

The MAX17595/MAX17596/MAX17597 devices implement soft-start operation for the flyback/boost regulator. A capacitor connected to the SS pin programs the soft-start period. The soft-start feature reduces input inrush current during startup. The devices allow the end user to select between voltage soft-start, usually preferred in nonisolated applications, and current soft-start, which is useful in isolated applications to get a monotonic and smooth rise in output voltage. See the *Input Voltage Range (V_{IN})* section.

Soft-Stop

A soft-stop feature can be requested from the factory. This feature ramps down the duty cycle of operation of the converter to zero in a controlled fashion, and enables controlled ramp down of output voltage. The soft-stop duration is twice that of the programmed soft-start period. This is particularly useful in implementing controlled shutdown of output voltage in isolated power converters.

Switching Frequency Selection (RT)

The ICs' switching frequency is programmable between 100kHz and 1MHz with a resistor R_{RT} connected between RT and SGND. Use the following formula to determine the appropriate value of R_{RT} needed to generate the desired output-switching frequency (f_{SW}):

$$R_{RT} = \frac{10^{10}}{f_{SW}}$$

where f_{SW} is the desired switching frequency.

Frequency Dithering for Spread-Spectrum Applications (Low EMI)

The switching frequency of the converter can be dithered in a range of ±10% by connecting a capacitor from DITHER/SYNC to SGND, and a resistor from DITHER to RT, as shown in the *Typical Operating Circuits*. Spread-spectrum modulation technique spreads the energy of switching frequency and its harmonics over a wider band while reducing their peaks, helping to meet stringent EMI goals.

Applications Information

Startup Voltage and Input Overvoltage Protection Setting (EN/UVLO, OVI)

The devices' EN/UVLO pin serves as an enable/disable input, as well as an accurate programmable input UVLO pin. The devices do not commence startup operation unless the EN/UVLO pin voltage exceeds 1.21V (typ). The devices turn off if the EN/UVLO pin voltage falls below 1.15V (typ). A resistor-divider from the input DC bus to ground can be used to divide down and apply a fraction of the input DC voltage (V_{DC}) to the EN/UVLO pin. The values of the resistor-divider can be selected so that the EN/UVLO pin voltage exceeds the 1.23V (typ) turn-on threshold at the desired input DC bus voltage. The same resistor-divider can be modified with an additional resistor (R_{OVI}) to implement input overvoltage protection in addition to the EN/UVLO functionality as shown in Figure 2. When voltage at the OVI pin exceeds 1.21V (typ), the devices stop switching and resume switching operations only if voltage at the OVI pin falls below 1.15V (typ). For given values of startup DC input

voltage (V_{START}) and input overvoltage-protection voltage (V_{OVI}), the resistor values for the divider can be calculated as follows, assuming a 24.9kΩ resistor for R_{OVI}:

$$R_{EN} = R_{OVI} \times \left[\frac{V_{OVI}}{V_{START}} - 1\right] k\Omega$$

where R_{OVI} is in kΩ, while V_{START} and V_{OVI} are in volts.

$$R_{SUM} = [R_{OVI} + R_{EN}] \times \left[\frac{V_{START}}{1.21} - 1\right] k\Omega$$

where R_{EN} , R_{OVI} is in kΩ, while V_{START} is in volts.

In universal AC input applications, R_{SUM} might need to be implemented as equal resistors in series (R_{DC1}, R_{DC2}, and R_{DC}) so that voltage across each resistor is limited to its maximum operation voltage.

$$R_{DC1} = R_{DC2} = R_{DC3} = \frac{R_{SUM}}{3} k\Omega$$

For low-voltage DC-DC applications based on the MAX17596/MAX17597, a single resistor can be used in the place of R_{SUM}, as the voltage across it is approximately 40V.

Startup Operation

The MAX17595 is optimized for implementing an offline single-switch flyback converter and has a 20V V_{IN} UVLO wake-up level with hysteresis of 15V (min). In offline applications, a simple cost-effective RC startup circuit is used. When the input DC voltage is applied, the startup resistor (R_{START}) charges the startup capacitor (C_{START}), causing the voltage at the V_{IN} pin to increase towards the wake-up V_{IN} UVLO threshold (20V typ). During this time, the MAX17595 draws a low startup current of 20µA (typ) through R_{START}. When the voltage at V_{IN} reaches the wake-up V_{IN} UVLO threshold, the MAX17595 commences switching and control operations. In this condition, the MAX17595 draws 2mA (typ) current from C_{START}, when operated at 1MHz switching frequency, for its internal operation. In addition, the average value of gate drive current is also drawn from C_{START}, which is a function of the gate charge of the external MOSFET used. Since this total current cannot be supported by the current through R_{START}, the voltage on C_{START} starts to drop. When suitably configured, as shown in Figure 9, the external MOSFET is switched by the NDRV pin and the flyback converter generates an output voltage

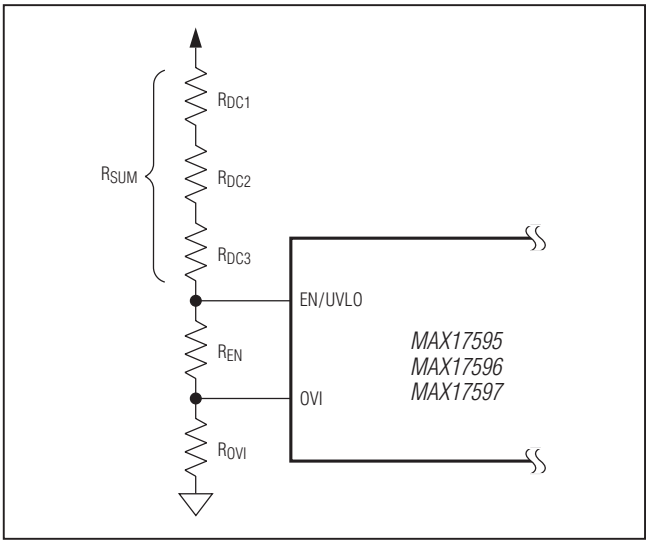


Figure 2. Programming EN/UVLO and OVI

(V_{OUT}), and a bias voltage (V_{BIAS}) that is bootstrapped to the V_{IN} pin through the diode (D2). If V_{BIAS} exceeds the sum of 7V, and the drop across D2 before the voltage on C_{START} falls below 7V, then the V_{IN} voltage is sustained by V_{BIAS}, allowing the MAX17595 to continue operating with energy from V_{BIAS}. The large hysteresis (13V typ) of the MAX17595 allows for a small startup capacitor (C_{START}). The low startup current (20µA typ) allows the use of a large startup resistor (R_{START}), thus reducing power dissipation at higher DC bus voltages. Figure 3 shows the typical RC startup scheme for the MAX17595, when the output voltage V_{OUT} is used as the bias voltage to sustain switching operation. R_{START} might need to be implemented as equal, multiple resistors in series (R_{IN1}, R_{IN2}, and R_{IN3}) to share the applied high DC voltage in offline applications so that the voltage across each resistor is limited to its maximum continuous operating voltage rating. R_{START} and C_{START} can be calculated as:

$$C_{START} = \left[I_{IN} + \left(\frac{Q_{GATE} \times f_{SW}}{10^6}\right)\right] \times \frac{t_{SS}}{10} \mu F$$

where I_{IN} is the supply current drawn at the V_{IN} pin in mA, Q_{GATE} is the gate charge of the external MOSFET used in nC, f_{SW} is the switching frequency of the converter in Hz, and t_{SS} is the soft-start time programmed for the flyback converter in ms. See the *Programming Soft-Start of Flyback/Boost Converter (SS)* section.

$$R_{START} = \frac{(V_{START} - 10) \times 50}{[1 + C_{START}]}\ k\Omega$$

where C_{START} is the startup capacitor in µF.

For designs that cannot accept power dissipation in the startup resistors at high DC input voltages in offline applications, the startup circuit can be set up with a current source instead of a startup resistor as shown in Figure 4.

The startup capacitor (C_{START}) can be calculated as:

$$C_{START} = \left[I_{IN} + \left(\frac{Q_{GATE} \times f_{SW}}{10^6} \right) \right] \times \frac{t_{SS}}{10}\ \mu F$$

where I_{IN} is the supply current drawn at the V_{IN} pin in mA, Q_{GATE} is the gate charge of the external MOSFET used in nC, f_{SW} is the switching frequency of the converter in kHz, and t_{SS} is the soft-start time programmed for the flyback converter in ms.

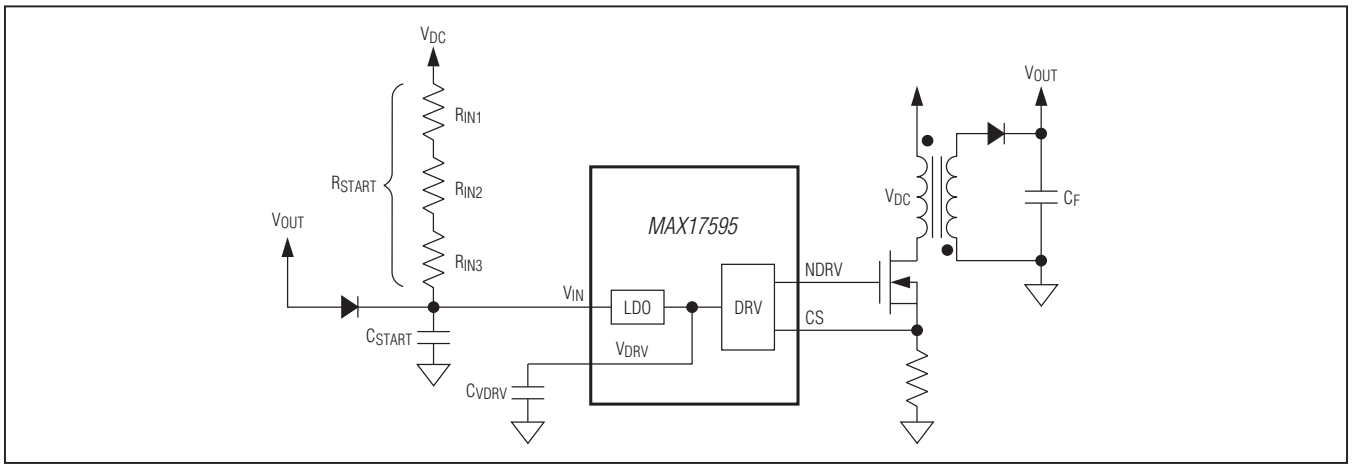


Figure 3. MAX17595 RC-Based Startup Circuit

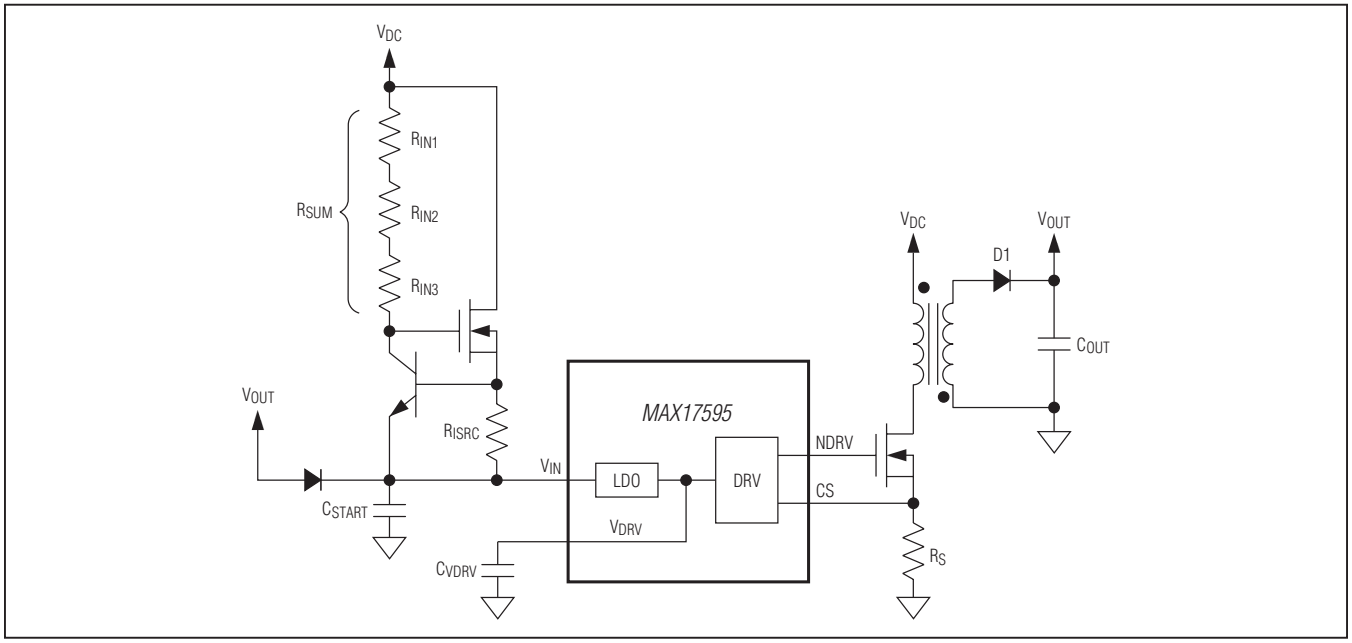


Figure 4. MAX17595 Current-Source-Based Startup Circuit

Resistors R_{SUM} and R_{ISRC} can be calculated as:

$$R_{SUM} = \frac{V_{START}}{10} M\Omega$$

$$R_{ISRC} = \frac{V_{BEQ1}}{70} M\Omega$$

The V_{IN} UVLO wakeup threshold of the MAX17596/MAX17597 is set to 4.1V (typ) with a 200mV hysteresis, optimized for low-voltage DC-DC applications down to 4.5V. For applications where the input DC voltage is low enough (e.g., 4.5V to 5.5V DC) that the power loss incurred to supply the operating current of the MAX17596/MAX17597 can be tolerated, the V_{IN} pin is directly connected to the DC input, as shown in Figure 5. In the case of higher DC input voltages (e.g., 16V to 32V DC), a startup circuit, such as that shown in Figure 6, can be used to minimize power dissipation in the startup circuit. In this startup scheme, the transistor (Q1) supplies the switching current until a bias winding NB comes up. The resistor (R_Z) can be calculated as:

$$R_Z = 9 \times (V_{INMIN} - 6.3)\ k\Omega$$

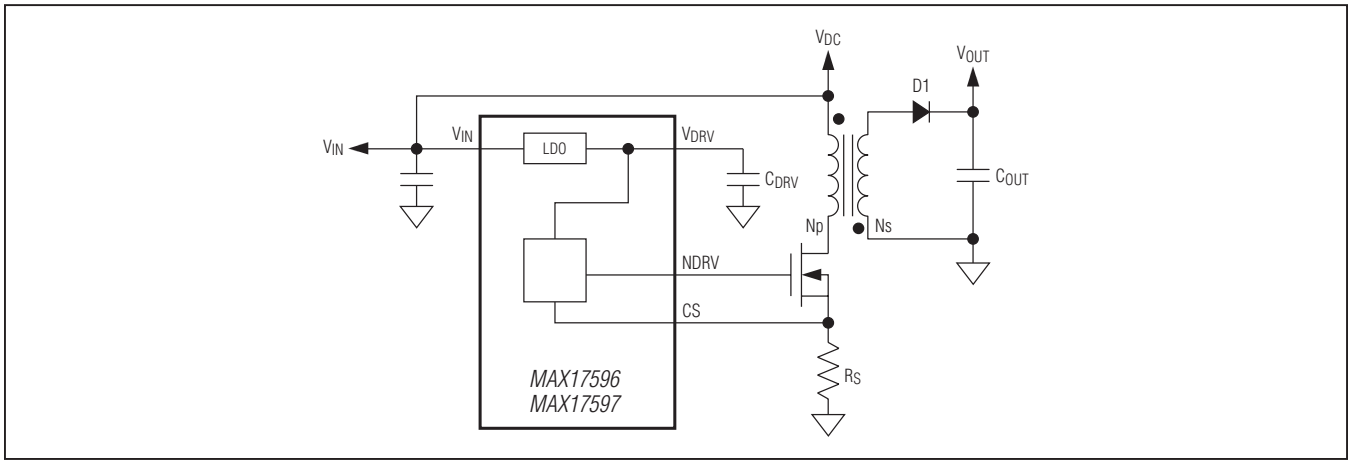


Figure 5. MAX17596/MAX17597 Typical Startup Circuit with V_{IN} Connected Directly to DC Input

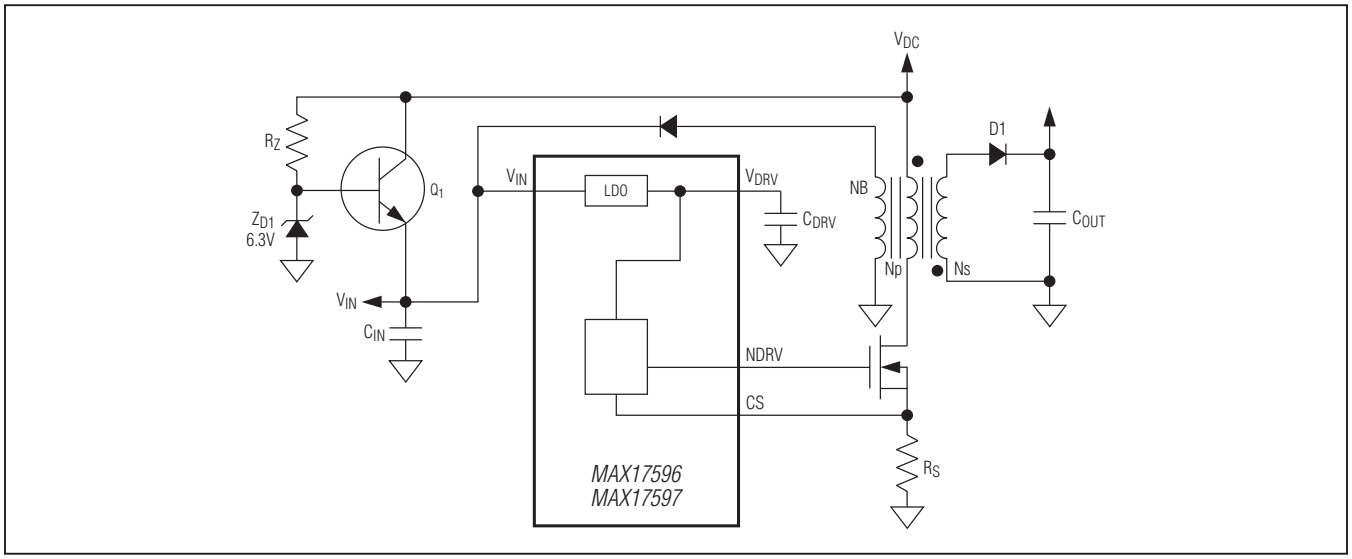


Figure 6. MAX17596/MAX17597 Typical Startup Circuit with Bias Winding to Turn Off Q1 and Reduce Power Dissipation

Programming Soft-Start of Flyback/Boost Converter (SS)

The soft-start period in the voltage soft-start scheme of the devices can be programmed by selecting the value of the capacitor connected from the SS pin to SGND. The capacitor C_{SS} can be calculated as:

$$C_{SS} = 8.2645 \times t_{SS}\ \text{nF}$$

where t_{SS} is expressed in ms. The soft-start period in the current soft-start scheme depends on the load at the output and the soft-start capacitor.

Programming Output Voltage

The devices incorporate an error amplifier with a 1% precision voltage reference that enables negative feedback control of the output voltage. The output voltage of the switching converter can be programmed by selecting the values for the resistor-divider connected from V_{OUT}, and the flyback/boost output to ground, with the midpoint of the divider connected to the FB pin (Figure 7). With R_B selected in the 20kΩ to 50kΩ range, R_U can be calculated as:

$$R_U = R_B \times \left[\frac{V_{OUT}}{1.21} - 1\right] \text{k}\Omega, \text{ where } R_B \text{ is in k}\Omega.$$

Peak-Current-Limit Setting (CS)

The devices include a robust overcurrent protection scheme that protects the device under overload and short-circuit conditions. A current-sense resistor (R_{CS} in the *Typical Operating Circuits*), connected between the source of the MOSFET and PGND, sets the peak current limit. The current-limit comparator has a voltage trip level ($V_{CS\text{-}PEAK}$) of 300mV. Use the following equation to calculate the value of R_{CS}:

$$R_{CS} = \frac{300\text{mV}}{I_{MOSFET}}\ \Omega$$

where I_{MOSFET} is the peak current flowing through the MOSFET. When the voltage produced by this current (through the current-sense resistor) exceeds the current-limit comparator threshold, the MOSFET driver (NDRV) terminates the current on-cycle within 30ns (typ).

The devices implement 65ns of leading-edge blanking to ignore leading-edge current spikes. These spikes are caused by reflected secondary currents, capacitance discharging current at the MOSFET's drain, and gate charging current. Use a small RC network for additional filtering of the leading edge spike on the sense waveform when needed. Set the corner frequency between 10MHz and 20MHz. After the leading-edge blanking time, the device monitors V_{CS}. The duty cycle is terminated immediately when V_{CS} exceeds 300mV.

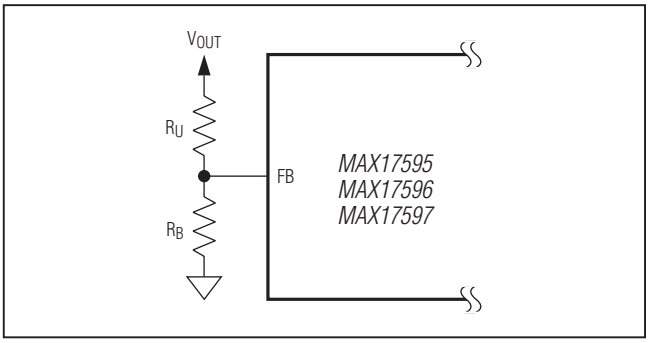


Figure 7. Programming Output Voltage

The devices offer a runaway current limit scheme that protects the devices under high-input-voltage short-circuit conditions when there is insufficient output voltage available to restore inductor current built up during the on period of the flyback/boost converter. Either eight consecutive occurrences of the peak-current-limit event or one occurrence of the runaway current limit trigger a hiccup mode that protects the converter by immediately suspending switching for a period of time (t_{RSTART}). This allows the overload current to decay due to power loss in the converter resistances, load, and the output diode of the flyback/boost converter before soft-start is attempted again. The runaway current limit is set at a $V_{CS\text{-}PEAK}$ of 360mV (typ). The peak-current-limit-triggered hiccup operation is disabled until the end of the soft-start period, while the runaway current-limit-triggered hiccup operation is always enabled.

Programming Slope Compensation (SLOPE)

The MAX17595/MAX17596 operate at a maximum duty cycle of 49%. In theory, they do not require slope compensation to prevent subharmonic instability that occurs naturally in continuous-conduction mode (CCM) peak-current-mode-controlled converters operating at duty cycles greater than 50%. In practice, the MAX17595/MAX17596 require a minimum amount of slope compensation to provide stable operation. The devices allow the user to program this default value of slope compensation simply by leaving the SLOPE pin unconnected. It is recommended that discontinuous-mode designs also use this minimum amount of slope compensation to provide better noise immunity and jitter-free operation.

The MAX17597 flyback/boost converter can be designed to operate in either discontinuous-conduction mode (DCM) or to enter into the continuous-conduction mode at a specific load condition for a given DC input voltage. In continuous-conduction mode, the flyback/boost converter needs slope compensation to avoid subharmonic instability that occurs naturally over all specified load and line conditions in peak-current-mode controlled converters operating at duty cycles greater than 50%. A minimum amount of slope signal is added to the sensed current signal even for converters operating below 50% duty to provide stable, jitter-free operation. The SLOPE pin allows the user to program the necessary slope compensation by setting the value of the resistor (R_{SLOPE}) connected from the SLOPE pin to ground.

$$R_{SLOPE} = \frac{S_E - 8}{1.55}\ k\Omega$$

where the slope (S_E) is expressed in mV/µs.

Frequency Dithering for Spread-Spectrum Applications (Low EMI)

The switching frequency of the converter can be dithered in a range of ±10% by connecting a capacitor from DITHER/SYNC to SGND, and a resistor from DITHER to RT as shown in the *Typical Operating Circuits*. This results in lower EMI.

A current source at DITHER/SYNC charges the capacitor C_{DITHER} to 2V at 50µA. Upon reaching this trip point, it discharges C_{DITHER} to 0.4V at 50µA. The charging and discharging of the capacitor generates a triangular waveform on DITHER/SYNC with peak levels at 0.4V and 2V and a frequency that is equal to:

$$f_{TRI} = \frac{50\mu A}{C_{DITHER} \times 3.2V}$$

typically, f_{TRI} should be set close to 1kHz. The resistor R_{DITHER} connected from DITHER/SYNC to RT determines the amount of dither as follows:

$$\%DITHER = \frac{R_{RT}}{R_{DITHER}}$$

where %DITHER is the amount of dither expressed as a percentage of the switching frequency. Setting R_{DITHER} to 10 x R_{RT} generates ±10% dither.

Error Amplifier, Loop Compensation, and Power Stage Design of Flyback/Boost Converter

The flyback/boost converter requires proper loop compensation to be applied to the error-amplifier output to achieve stable operation. The goal of the compensator design is to achieve desired closed-loop bandwidth, and sufficient phase margin at the crossover frequency of the open-loop gain-transfer function of the converter. The error amplifier provided in the devices is a transconductance amplifier. The compensation network used to apply the necessary loop compensation is shown in Figure 8.

The flyback/boost converter can be used to implement the following converters and operating modes:

- Nonisolated flyback converter in discontinuous-conduction mode (DCM flyback)
- Nonisolated flyback converter in continuous-conduction mode (CCM flyback)
- Boost converter in discontinuous-conduction mode (DCM boost)
- Boost converter in continuous-conduction mode (CCM boost)

Calculations for loop-compensation values (R_Z, C_Z, and C_P) for these converter types and design procedures for power-stage components are detailed in the following sections.

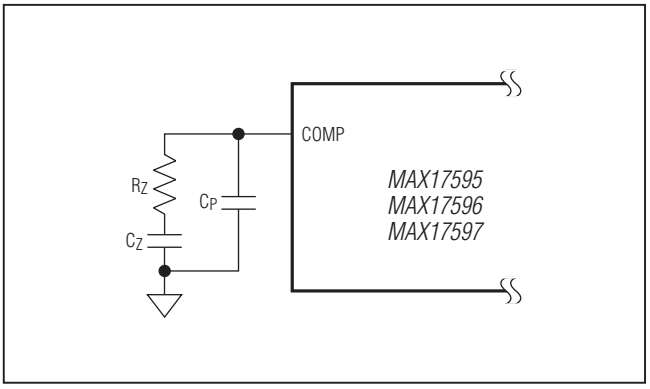


Figure 8. Error-Amplifier Compensation Network

DCM Flyback

Primary Inductance Selection

In a DCM flyback converter, the energy stored in the primary inductance of the flyback transformer is delivered entirely to the output. The maximum primary inductance value for which the converter remains in DCM at all operating conditions can be calculated as:

$$L_{PRIMAX} \le \frac{(V_{INMIN} \times D_{MAX})^2 \times 0.4}{(V_{OUT} + V_D) \times I_{OUT} \times f_{SW}}$$

where D_{MAX} is chosen as 0.35 for the MAX17595/MAX17596 and 0.7 for the MAX17597; V_D is the voltage drop of the output rectifier diode on the secondary winding, and f_{SW} is the switching frequency of the power converter. Choose the primary inductance value to be less than L_{PRIMAX}.

Duty Cycle Calculation

The accurate value of the duty cycle (D_{NEW}) for the selected primary inductance (L_{PRI}) can be calculated using the following equation:

$$D_{NEW} = \frac{\sqrt{2.5 \times L_{PRI} \times (V_{OUT} + V_D) \times I_{OUT} \times f_{SW}}}{V_{INMIN}}$$

Turns Ratio Calculation (Ns/Np)

Transformer turns ratio (K = Ns/Np) can be calculated as:

$$K = \frac{(V_{OUT} + V_D) \times (1 - D_{MAX})}{V_{INMIN} \times D_{MAX}}$$

Peak/RMS Current Calculation

The transformer manufacturer needs RMS current values in the primary and secondary to design the wire diameter for the different windings. Peak current calculations are useful in setting the current limit. Use the following equations to calculate the primary and secondary peak and RMS currents.

Maximum primary peak current:

$$I_{PRIPEAK} = \frac{V_{INMIN} \times D_{NEW}}{L_{PRI} \times f_{SW}}$$

Maximum primary RMS current:

$$I_{PRIRMS} = I_{PRIPEAK} \times \sqrt{\frac{D_{NEW}}{3}}$$

Maximum secondary peak current:

$$I_{SECPEAK} = \frac{I_{PRIPEAK}}{K}$$

Maximum primary peak current:

$$I_{SECRMS} = I_{PRIPEAK} \sqrt{\frac{I_{SECPEAK} \times L_{PRI} \times f_{SW}}{3 \times (V_{OUT} + V_D)}}$$

For the purpose of current-limit setting, I_{LIM} can be calculated as follows:

$$I_{LIM} = I_{PRIPEAK} \times 1.2$$

Primary Snubber Selection

Ideally, the external MOSFET experiences a drain-source voltage stress equal to the sum of the input voltage and reflected voltage across the primary winding during the off period of the MOSFET. In practice, parasitic inductors and capacitors in the circuit, such as leakage inductance of the flyback transformer, cause voltage overshoot and ringing, in addition to the ideally expected voltage stress. Snubber circuits are used to limit the voltage overshoots to safe levels within the voltage rating of the external MOSFET. The snubber capacitor can be calculated using the following equation:

$$C_{SNUB} = \frac{2 \times L_{LK} \times I_{PRIPEAK}^2 \times K^2}{V_{OUT}^2}$$

where L_{LK} is the leakage inductance that can be obtained from the transformer specifications (usually 1.5%–2% of the primary inductance).

The power to be dissipated in the snubber resistor is calculated using the following formula:

$$P_{SNUB} = 0.833 \times L_{LK} \times I_{PRIPEAK}^2 \times f_{SW}$$

The snubber resistor is calculated based on the equation below:

$$R_{SNUB} = \frac{6.25 \times V_{OUT}^2}{P_{SNUB} \times K^2}$$

The voltage rating of the snubber diode is:

$$V_{DSNUB} = V_{INMAX} + \left(2.5 \times \frac{V_{OUT}}{K}\right)$$

Output Capacitor Selection

X7R ceramic output capacitors are preferred in industrial applications due to their stability over temperature. The output capacitor is usually sized to support a step load of 50% of the maximum output current in the application, so that the output-voltage deviation is contained to 3% of the output-voltage change. The output capacitance can be calculated as follows:

$$C_{OUT} = \frac{I_{STEP} \times t_{RESPONSE}}{\Delta V_{OUT}}$$

$$t_{RESPONSE} \cong \left[\frac{0.33}{f_C} + \frac{1}{f_{SW}}\right]$$

where I_{STEP} is the load step, $t_{RESPONSE}$ is the response time of the controller, ΔV_{OUT} is the allowable output voltage deviation, and f_C is the target closed-loop crossover frequency. f_C is chosen to be one-tenth of the switching frequency, f_{SW}. For the flyback converter, the output capacitor supplies the load current when the main switch is on; therefore, the output voltage ripple is a function of load current and duty cycle. Use the following equation to calculate the output capacitor ripple:

$$\Delta V_{COUT} = \frac{D_{NEW} \times \left[I_{PRIPEAK} - \left[K \times I_{OUT}\right]\right]^2}{2 \times I_{PRIPEAK} \times f_{SW} \times C_{OUT}}$$

where I_{OUT} is load current and D_{NEW} is the duty cycle at minimum input voltage.

Input Capacitor Selection

The MAX17595 is optimized to implement offline AC-DC converters. In such applications, the input capacitor must be selected based on either the ripple due to the rectified line voltage, or based on holdup-time requirements. Holdup time can be defined as the time period over which the power supply should regulate its output voltage from the instant the AC power fails. The MAX17596/MAX17597 are useful in implementing low-voltage DC-DC applications where the switching-frequency ripple must be used to calculate the input capacitor. In both cases, the capacitor must be sized to meet RMS current requirements for reliable operation.

A) **Capacitor selection based on switching ripple (MAX17596/MAX17597)**

For DC-DC applications, X7R ceramic capacitors are recommended due to their stability over the operating temperature range. The ESR and ESL of a ceramic capacitor are relatively low, so the ripple voltage is dominated by the capacitive component. For the flyback converter, the input capacitor supplies the current when the main switch is on. Use the following equation to calculate the input capacitor for a specified peak-to-peak input switching ripple (V_{IN_RIP}):

$$C_{IN} = \frac{D_{NEW} \times I_{PRIPEAK}\left[1 - (0.5 \times D_{NEW})\right]^2}{2 \times f_{SW} \times V_{IN_RIP}}$$

B) **Capacitor selection based on rectified line voltage ripple (MAX17595)**

For the flyback converter, the input capacitor supplies the input current when the diode rectifier is off. The voltage discharge (V_{IN_RIP}), due to the input average current, should be within the limits specified:

$$C_{IN} = \frac{0.5 \times I_{PRIPEAK} \times D_{NEW}}{f_{RIPPLE} \times V_{IN_RIP}}$$

where f_{RIPPLE}, the input AC ripple frequency equal to the supply frequency for half-wave rectification, is two times the AC supply frequency for full-wave rectification.

C) **Capacitor selection based on holdup time requirements (MAX17595)**

For a given output power (P_{HOLDUP}) that needs to be delivered during holdup time (t_{HOLDUP}), DC bus voltage at which the AC supply fails (V_{INFAIL}), and the minimum DC bus voltage at which the converter can regulate the output voltages (V_{INMIN}), the input capacitor (C_{IN}) is estimated as:

$$C_{IN} = \frac{3 \times P_{HOLDUP} \times t_{HOLDUP}}{(V_{INFAIL}^2 - V_{INMIN}^2)}$$

the input capacitor RMS current can be calculated as:

$$I_{INCRMS} = \frac{0.6 \times V_{INMIN} \times (D_{MAX})^2}{f_{SW} \times L_{PRI}}$$

External MOSFET Selection

A MOSFET selection criterion includes maximum drain voltage, peak/RMS current in the primary, and the maximum allowable power dissipation of the package without exceeding the junction temperature limits. The voltage seen by the MOSFET drain is the sum of the input voltage, the reflected secondary voltage on the transformer primary, and the leakage inductance spike. The MOSFET's absolute maximum V_{DS} rating must be higher than the worst-case drain voltage:

$$V_{DSMAX} = V_{INMAX} + \left[\left(\frac{V_{OUT} + V_{DIODE}}{K}\right) \times 2.5\right]$$

The drain current rating of the external MOSFET is selected to be greater than the worst-case peak-current-limit setting.

Secondary Diode Selection

Secondary-diode selection criteria includes the maximum reverse voltage, average current in the secondary-reverse recovery time, junction capacitance, and the maximum allowable power dissipation of the package. The voltage stress on the diode is the sum of the output voltage and the reflected primary voltage. The maximum operating reverse-voltage rating must be higher than the worst-case reverse voltage:

$$V_{SECDIODE} = 1.25 \times (K \times V_{INMAX} + V_{OUT})$$

The current rating of the secondary diode should be selected so that the power loss in the diode (given as the product of forward-voltage drop and the average diode current) should be low enough to ensure that the junction temperature is within limits. This necessitates that the diode current rating be in the order of 2 x I_{OUT} to 3 x I_{OUT}. Select fast-recovery diodes with a recovery time less than 50ns, or Schottky diodes with low junction capacitance.

Error Amplifier Compensation Design

The loop compensation values are calculated as:

$$R_Z = 450 \times \sqrt{\frac{\left[1 + \left[\frac{0.1 \times f_{SW}}{f_P}\right]^2\right] \times V_{OUT} \times I_{OUT}}{2 \times L_{PRI} \times f_{SW}}}$$

where:

$$f_P = \frac{I_{OUT}}{\pi \times V_{OUT} \times C_{OUT}}$$

$$C_Z = \frac{1}{\pi \times R_Z \times f_P}$$

$$C_P = \frac{1}{\pi \times R_Z \times f_{SW}}$$

f_{SW} is the switching frequency of the devices.

CCM Flyback

Transformer Turns Ratio Calculation (K = Ns/Np)

The transformer turns ratio can be calculated using the following formula:

$$K = \frac{(V_{OUT} + V_D) \times (1 - D_{MAX})}{V_{INMIN} \times D_{MAX}}$$

where D_{MAX} is the duty cycle assumed at minimum input (0.35 for the MAX17595/MAX17596 and 0.7 for the MAX17597).

Primary Inductance Calculation

Calculate the primary inductance based on the ripple:

$$L_{PRI} = \frac{(V_{OUT} + V_D) \times (1 - D_{NOM}) \times K}{2 \times I_{OUT} \times \beta \times f_{SW}}$$

where D_{NOM}, the nominal duty cycle at nominal operating DC input voltage V_{INNOM}, is given as:

$$D_{NOM} = \frac{(V_{OUT} + V_D) \times K}{\left[V_{INNOM} + (V_{OUT} + V_D) \times K\right]}$$

The output current, down to which the flyback converter should operate in CCM, is determined by selection of the fraction ß in the above primary inductance formula. For example, ß should be selected as 0.15 so that the converter operates in CCM down to 15% of the maximum output load current. Since the ripple in the primary current waveform is a function of duty cycle and is maximum at maximum DC input voltage, the maximum (worst-case) load current down to which the converter operates in CCM occurs at maximum operating DC input voltage. V_D is the forward drop of the selected output diode at maximum output current.

Peak and RMS Current Calculation

RMS current values in the primary and secondary are needed by the transformer manufacturer to design the wire diameter for the different windings. Peak current calculations are useful in setting the current limit. Use the following equations to calculate the primary and secondary peak and RMS currents.

Maximum primary peak current:

$$I_{PRIPEAK} = \left(\frac{I_{OUT} \times K}{1 - D_{MAX}}\right) + \left(\frac{V_{INMIN} \times D_{MAX}}{2 \times L_{PRI} \times f_{SW}}\right)$$

Maximum primary RMS current:

$$I_{PRIRMS} = \sqrt{\frac{I_{PRIPEAK}^2 + \Delta I_{PRI}^2 - (I_{PRIPEAK} \times \Delta I_{PRI})}{3}} \times \sqrt{D_{MAX}}$$

where ΔI_{PRI} is the ripple current in the primary current waveform and is given by:

$$\Delta I_{PRI} = \left(\frac{V_{INMIN} \times D_{MAX}}{L_{PRI} \times f_{SW}}\right)$$

Maximum secondary peak current:

$$I_{SECPEAK} = \frac{I_{PRIPEAK}}{K}$$

Maximum secondary RMS current:

$$I_{SECRMS} = \sqrt{\frac{I_{SECPEAK}^2 + \Delta I_{SEC}^2 + (I_{SECPEAK} \times \Delta I_{SEC})}{3}} \times \sqrt{1 - D_{MAX}}$$

where ΔI_{SEC} is the ripple current in the secondary current waveform and is given by:

$$\Delta I_{SEC} = \left(\frac{V_{INMIN} \times D_{MAX}}{L_{PRI} \times f_{SW} \times K}\right)$$

For the purpose of current-limit setting, the peak current can be calculated as follows:

$$I_{LIM} = I_{PRIPEAK} \times 1.2$$

Primary RCD Snubber Selection

The design procedure for primary RCD snubber selection is identical to that outlined in the *DCM Flyback* section.

Output Capacitor Selection

X7R ceramic output capacitors are preferred in industrial applications due to their stability over temperature. The output capacitor is usually sized to support a step load of 50% of the maximum output current in the application so that the output-voltage deviation is contained to 3% of the output-voltage change. The output capacitance can be calculated as:

$$C_{OUT} = \frac{I_{STEP} \times t_{RESPONSE}}{\Delta V_{OUT}}$$

$$t_{RESPONSE} \cong \left(\frac{0.33}{f_C} + \frac{1}{f_{SW}}\right)$$

where I_{STEP} is the load step, $t_{RESPONSE}$ is the response time of the controller, ΔV_{OUT} is the allowable output voltage deviation, and f_C is the target closed-loop cross-over frequency. f_C is chosen to be less than one-fifth of the worst-case (lowest) RHP zero frequency f_{RHP}. The right half-plane zero frequency is calculated as follows:

$$f_{ZRHP} = \frac{(1 - D_{MAX})^2 \times V_{OUT}}{2 \times \pi \times D_{MAX} \times L_{PRI} \times I_{OUT} \times K^2}$$

For the CCM flyback converter, the output capacitor supplies the load current when the main switch is on; therefore, the output voltage ripple is a function of load current and duty cycle. Use the following equation to estimate the output voltage ripple:

$$\Delta V_{COUT} = \frac{I_{OUT} \times D_{MAX}}{f_{SW} \times C_{OUT}}$$

Input Capacitor Selection

The design procedure for input capacitor selection is identical to that outlined in the *DCM Flyback* section.

External MOSFET Selection

The design procedure for external MOSFET selection is identical to that outlined in the *DCM Flyback* section.

Secondary-Diode Selection

The design procedure for secondary-diode selection is identical to that outlined in the *DCM Flyback* section.

Error Amplifier Compensation Design

In the CCM flyback converter, the primary inductance and the equivalent load resistance introduces a right half-plane zero at the following frequency:

$$f_{ZRHP} = \frac{(1 - D_{MAX})^2 \times V_{OUT}}{2 \times \pi \times D_{MAX} \times L_{PRI} \times I_{OUT} \times K^2}$$

The loop compensation values are calculated as:

$$R_Z = \frac{225 \times I_{OUT}}{(1 - D_{MAX})} \times \sqrt{1 + \left[\frac{f_{RHP}}{5 \times f_P}\right]^2}$$

where f_P, the pole due to output capacitor and load is given by:

$$f_P = \frac{(1 + D_{MAX}) \times I_{OUT}}{2 \times \pi \times C_{OUT} \times V_{OUT}}$$

The above selection of R_Z sets the loop-gain crossover frequency (f_C, where the loop gain equals 1) equal to 1/5th the right half-plane zero frequency.

$$f_C \le \frac{f_{ZRHP}}{5}$$

With the control loop zero placed at the load pole frequency:

$$C_Z = \frac{1}{2\pi \times R_Z \times f_P}$$

With the high-frequency pole placed at half the switching frequency:

$$C_P = \frac{1}{\pi \times R_Z \times f_{SW}}$$

DCM Boost

In a DCM boost converter, the inductor current returns to zero in every switching cycle. Energy stored during the on-time of the main switch Q1 is delivered entirely to the load in each switching cycle.

Inductance Selection

The design procedure starts with calculating the boost converter's input inductor, such that it operates in DCM at all operating line and load conditions. The critical inductance required to maintain DCM operation is calculated as:

$$L_{IN} \le \frac{\left[\left(V_{OUT} - V_{IN_MIN}\right) \times V_{IN_MIN}^2\right] \times 0.4}{I_{OUT} \times V_{OUT}^2 \times f_{SW}}$$

where V_{INMIN} is the minimum input voltage.

Peak/RMS Currents Calculation

For the purposes of setting the current limit, the peak current in the inductor can be calculated as:

$$I_{LIM} = I_{PK} \times 1.2$$

where is I_{PK} given by:

$$I_{PK} = \sqrt{\left[\frac{2 \times (V_{OUT} - V_{IN_MIN}) \times I_{OUT}}{L_{INMIN} \times f_{SW}}\right]}$$

L_{INMIN} is the minimum value of the input inductor taking into account tolerance and saturation effects.

Output Capacitor Selection

The output capacitance can be calculated as follows:

$$C_{OUT} = \frac{I_{STEP} \times t_{RESPONSE}}{\Delta V_{OUT}}$$

$$t_{RESPONSE} \cong \left(\frac{0.33}{f_C} + \frac{1}{f_{SW}}\right)$$

where I_{STEP} is the load step, $t_{RESPONSE}$ is the response time of the controller, ΔV_{OUT} is the allowable output voltage deviation, and f_C is the target closed-loop crossover frequency. f_C is chosen to be one-tenth of the switching frequency f_{SW}. For the boost converter, the output capacitor supplies the load current when the main switch is on; therefore, the output voltage ripple is a function of duty cycle and load current. Use the following equation to calculate the output capacitor ripple:

$$\Delta V_{COUT} = \frac{I_{OUT} \times L_{IN} \times I_{PK}}{V_{INMIN} \times C_{OUT}}$$

Input Capacitor Selection

The input ceramic capacitor value required can be calculated based on the ripple allowed on the input DC bus. The input capacitor should be sized based on the RMS value of the AC current handled by it. The calculations are:

$$C_{IN} = \left[\frac{3.75 \times I_{OUT}}{V_{INMIN} \times f_{SWMIN} \times (1 - D_{MAX})}\right]$$

The capacitor RMS can be calculated as:

$$I_{CIN_RMS} = \frac{I_{PK}}{2 \times \sqrt{3}}$$

Error Amplifier Compensation Design

The loop compensation values for the error amplifier can now be calculated as:

$$C_Z = \frac{G_{DC} \times G_M \times 10}{2 \times \pi \times f_{SW}} = \left(G_{DC} \times 10\right) \text{nF}$$

where G_{DC}, the DC gain of the power stage, is given as:

$$G_{DC} = \sqrt{\frac{8 \times (V_{OUT} - V_{INMIN}) \times f_{SW} \times V_{OUT}^2 \times L_{IN}}{(2V_{OUT} - V_{INMIN})^2 \times I_{OUT}}}$$

$$R_Z = \frac{V_{OUT} \times C_{OUT} \times (V_{OUT} - V_{INMIN})}{I_{OUT} \times C_Z \times (2V_{OUT} - V_{INMIN})}$$

where V_{INMIN} is the minimum operating input voltage, and I_{OUT} is the maximum load current.

$$C_P = \frac{C_{OUT} \times ESR}{R_Z}$$

Slope Compensation

In theory, the DCM boost converter does not require slope compensation for stable operation. In practice, the converter needs a minimum amount of slope for good noise immunity at very light loads. The minimum slope is set for the MAX17596/MAX17597 by leaving the SLOPE pin unconnected.

Output Diode Selection

The voltage rating of the output diode for the boost converter ideally equals the output voltage of the boost converter. In practice, parasitic inductances and capacitances in the circuit interact to produce voltage overshoot during the turn-off transition of the diode that occurs when the main switch Q1 turns on. The diode rating should therefore be selected with the necessary margin to accommodate this extra voltage stress. A voltage rating of 1.3 x V_{OUT} provides the necessary design margin in most cases.

The current rating of the output diode should be selected so that the power loss in the diode (given as the product of forward-voltage drop and the average diode current) should be low enough to ensure that the junction temperature is within limits. This necessitates the diode current rating to be in the order of 2 x I_{OUT} to 3 x I_{OUT}. Select fast-recovery diodes with a recovery time less than 50ns or Schottky diodes with low junction capacitance.

MOSFET RMS Current Calculation

The voltage stress on the MOSFET ideally equals the sum of the output voltage and the forward drop of the output diode. In practice, voltage overshoot and ringing occur due to action of circuit parasitic elements during the turn-off transition. The MOSFET voltage rating should be selected with the necessary margin to accommodate this extra voltage stress. A voltage rating of 1.3 x V_{OUT} provides the necessary design margin in most cases.

The RMS current in the MOSFET is useful in estimating the conduction loss, and is given as:

$$I_{MOSFETRMS} = \sqrt{\frac{I_{PK}^3 \times L_{INS} \times f_{SW}}{3 \times V_{INMIN}}}$$

where I_{PK} is the peak current calculated at the lowest operating input voltage, V_{INMIN}.

CCM Boost

In a CCM boost converter, the inductor current does not return to zero during a switching cycle. Since the MAX17597 implements a nonsynchronous boost converter, the inductor current will enter DCM operation at load currents below a critical value equal to half of the peak-peak ripple in the inductor current.

Inductor Selection

The design procedure starts with calculating the boost converter's input inductor at nominal input voltage for a ripple in the inductor current equal to 30% of the maximum input current.

$$L_{IN} = \frac{V_{IN} \times D \times (1 - D)}{0.3 \times I_{OUT} \times f_{SW}}$$

where D is the duty cycle calculated as:

$$D = \frac{V_{OUT} + V_D - V_{IN}}{V_{OUT} + V_D - (R_{DS} \times I_{OUT})}$$

V_D is the voltage drop across the output diode of the boost converter at maximum output current, and R_{DS} is the resistance of the MOSFET in the on state.

Peak/RMS Current Calculation

For the purposes of setting the current limit, the peak current in the inductor and MOSFET can be calculated as follows:

$$I_{PK} = \left[\frac{V_{OUT} \times D_{MAX} \times (1 - D_{MAX})}{L_{INMIN} \times f_{SW}} + \frac{I_{OUT}}{(1 - D)}\right] \times 1.2 \text{ for } D_{MAX} < 0.5$$

$$\text{And, } I_{PK} = \left[\frac{0.25 \times V_{OUT}}{L_{INMIN} \times f_{SW}} + \frac{I_{OUT}}{(1 - D)}\right] \times 1.2 \text{ for } D_{MAX} \geq 0.5$$

D_{MAX}, the maximum duty cycle, is obtained by substituting the minimum input operating voltage V_{INMIN} in the equation above for duty cycle. L_{INMIN} is the minimum value of the input inductor taking into account tolerance and saturation effects.

Output Capacitor Selection

The output capacitance can be calculated as follows:

$$C_{OUT} = \frac{I_{STEP} \times t_{RESPONSE}}{\Delta V_{OUT}}$$

$$t_{RESPONSE} \cong \left(\frac{0.33}{f_C} + \frac{1}{f_{SW}}\right)$$

where I_{STEP} is the load step, $t_{RESPONSE}$ is the response time of the controller, ΔV_{OUT} is the allowable output voltage deviation, and f_C is the target closed-loop crossover frequency. f_C is chosen to be one-tenth of the switching frequency f_{SW}. For the boost converter, the output capacitor supplies the load current when the main switch is on; therefore, the output voltage ripple is a function of duty cycle and load current. Use the following equation to calculate the output capacitor ripple:

$$\Delta V_{COUT} = \frac{I_{OUT} \times D_{MAX}}{C_{OUT} \times f_{SW}}$$

Input Capacitor Selection

The input ceramic capacitor value required can be calculated based on the ripple allowed on the input DC bus. The input capacitor should be sized based on the RMS value of the AC current handled by it. The calculations are:

$$C_{IN} = \left[\frac{3.75 \times I_{OUT}}{V_{INMIN} \times f_{SW} \times (1 - D_{MAX})}\right]$$

The input capacitor RMS current can be calculated as:

$$I_{CIN_RMS} = \frac{\Delta I_{LIN}}{2 \times \sqrt{3}}$$

where:

$$\Delta I_{LIN} = \left[\frac{V_{OUT} \times D_{MAX} \times (1 - D_{MAX})}{L_{INMIN} \times f_{SW}}\right]$$

for $D_{MAX} < 0.5$,

$$\Delta I_{LIN} = \left[\frac{0.25 \times V_{OUT}}{L_{INMIN} \times f_{SW}}\right]$$

for $D_{MAX} \geq 0.5$

Error Amplifier Compensation Design

The loop compensation values for the error amplifier can now be calculated as:

$$R_Z = \frac{250 \times V_{OUT}^2 \times C_{OUT} \times (1 - D_{MIN})}{I_{OUTMIN} \times L_{IN}}$$

where D_{MIN} is the duty cycle at the highest operating input voltage, and I_{OUTMIN} is the minimum load current.

$$C_Z = \frac{V_{OUT} \times C_{OUT}}{2 \times I_{OUT} \times R_Z}$$

$$C_P = \frac{1}{\pi \times f_{SW} \times R_Z}$$

Slope Compensation Ramp

The slope required to stabilize the converter at duty cycles greater than 50% can be calculated as follows:

$$S_E = \frac{0.5 \times (0.82 \times V_{OUT} - V_{INMIN})}{L_{IN}} \text{ V/µs},$$

where L_{IN} is in µH.

Output Diodes Selection

The design procedure for output-diode selection is identical to that outlined in the *DCM Boost* section.

MOSFET RMS Current Calculation

The voltage stress on the MOSFET ideally equals the sum of the output voltage and the forward drop of the output diode. In practice, voltage overshoot and ringing occur due to action of circuit parasitic elements during the turn-off transition. The MOSFET voltage rating should be selected with the necessary margin to accommodate this extra voltage stress. A voltage rating of 1.3 x V_{OUT} provides the necessary design margin in most cases. The RMS current in the MOSFET is useful in estimating the conduction loss, and is given as:

$$I_{MOSFETRMS} = \frac{I_{OUT} \times \sqrt{D_{MAX}}}{(1 - D_{MAX})}$$

where D_{MAX} is the duty cycle at the lowest operating input voltage, and I_{OUT} is the maximum load current.

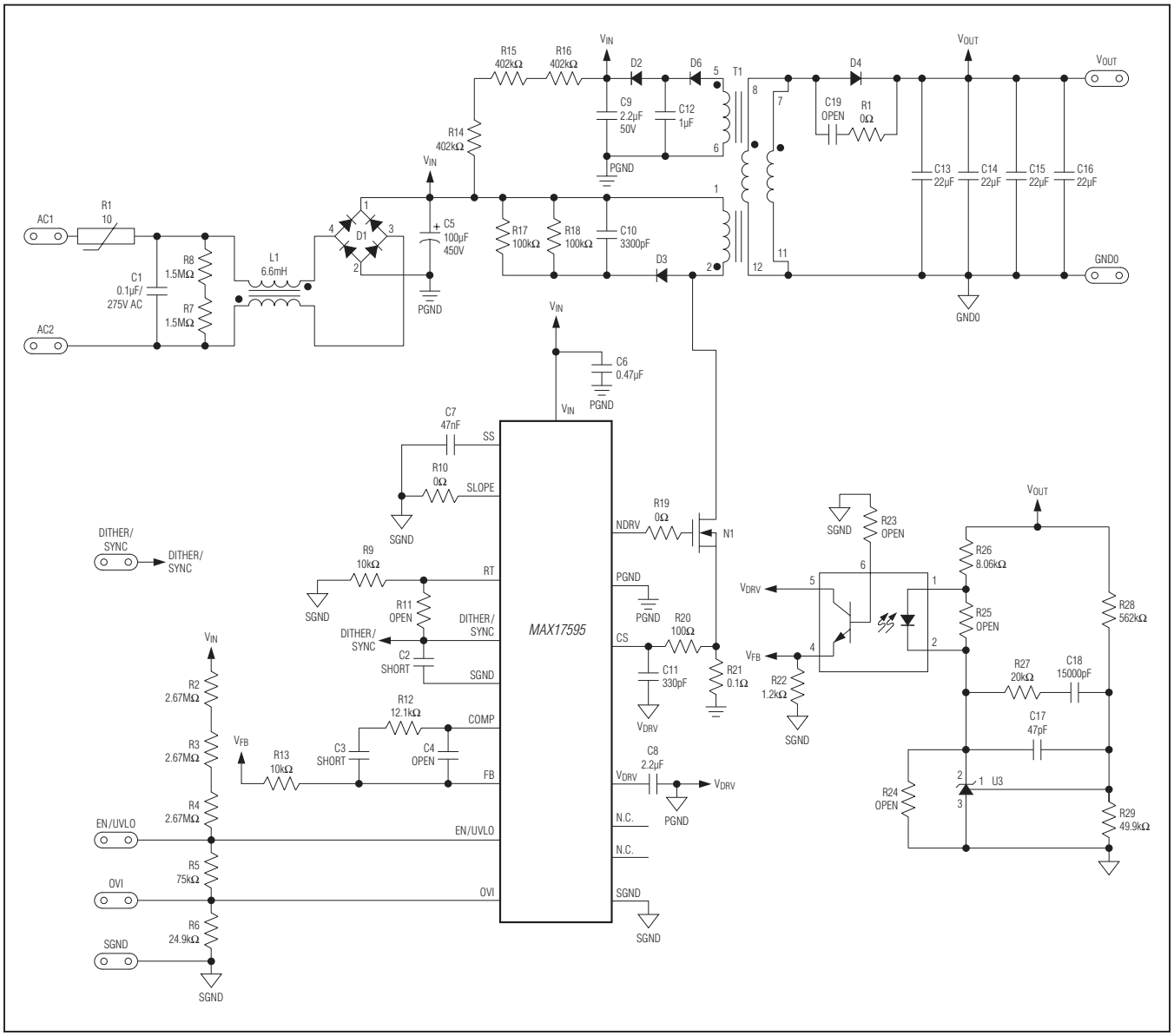


Figure 9. MAX17595 Typical Application Circuit (Universal Offline Isolated Power Supply)

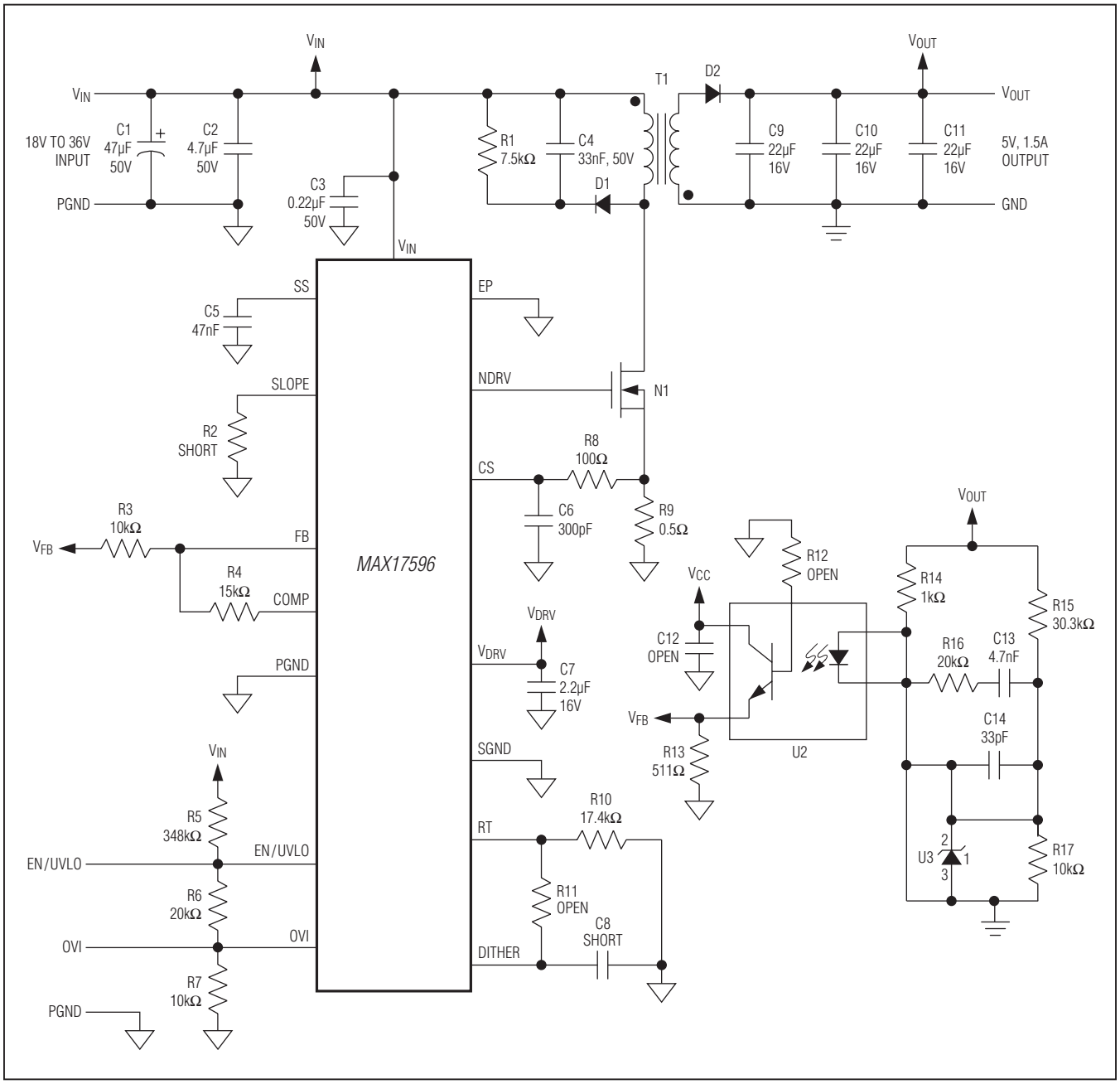


Figure 10. MAX17596 Typical Application Circuit (Power Supply for DC-DC Applications)

Typical Operating Circuits (continued)

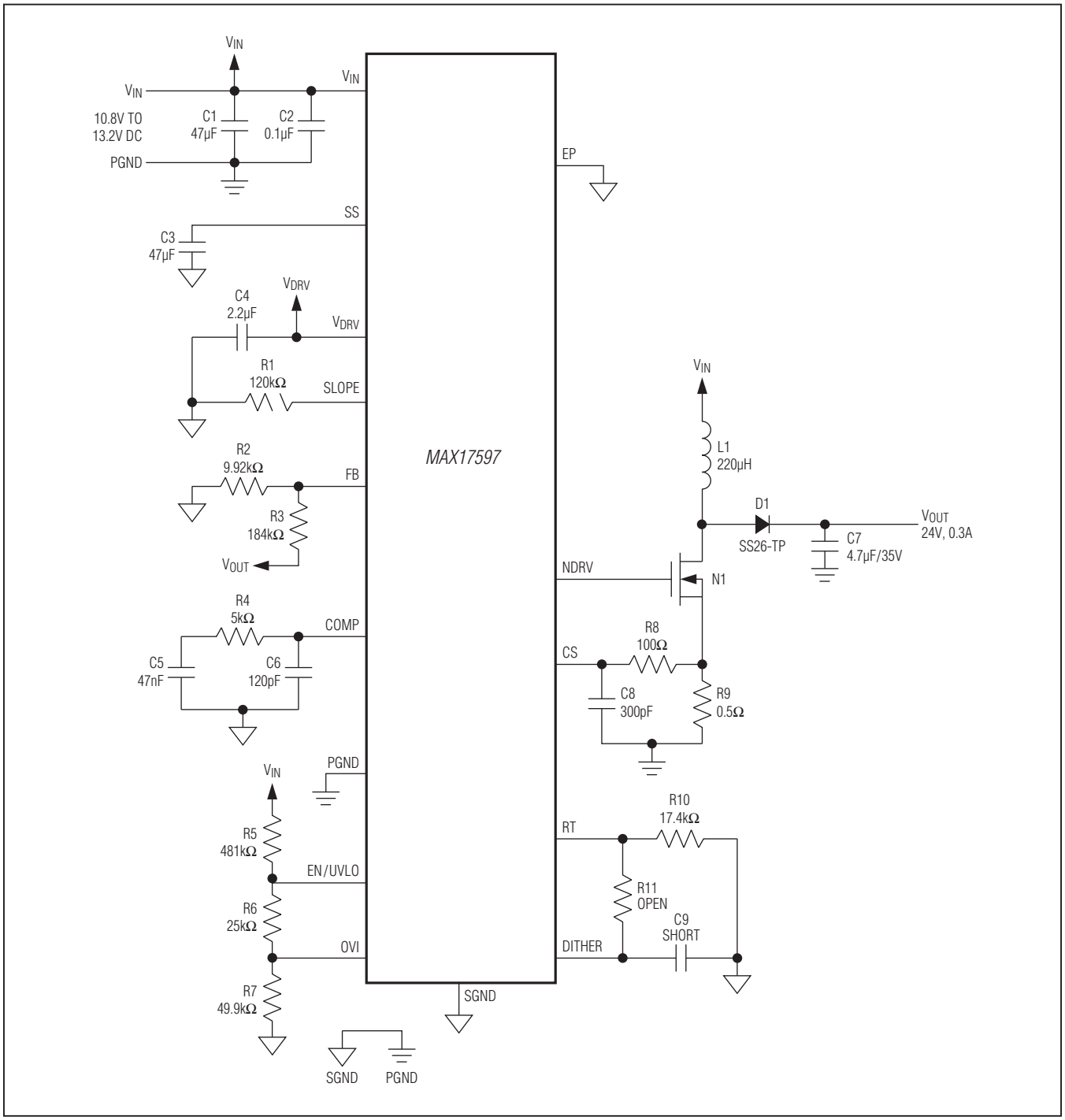


Figure 11. MAX17597 Typical Application Circuit (Nonsynchronous Boost Converter)

Layout, Grounding and Bypassing

All connections carrying pulsed currents must be very short and as wide as possible. The inductance of these connections must be kept to an absolute minimum due to the high di/dt of the currents in high-frequency-switching power converters. This implies that the loop areas for forward and return pulsed currents in various parts of the circuit should be minimized. Additionally, small current loop areas reduce radiated EMI. Similarly, the heatsink of the MOSFET presents a dV/dt source; therefore, the surface area of the MOSFET heatsink should be minimized as much as possible.

Ground planes must be kept as intact as possible. The ground plane for the power section of the converter should be kept separate from the analog ground plane, except for a connection at the least noisy section of the power ground plane, typically the return of the input filter capacitor. The negative terminal of the filter capacitor, the ground return of the power switch and current sensing resistor, must be close together. PCB layout also affects the thermal performance of the design. A number of thermal vias that connect to a large ground plane should be provided under the exposed pad of the part for efficient heat dissipation. For a sample layout that ensures first-pass success, refer to the MAX17595 evaluation kit layout available at **www.maxim-ic.com**. For universal AC input designs, follow all applicable safety regulations. Offline power supplies can require UL, VDE, and other similar agency approvals.

Ordering Information/Selector Guide

PART	TEMP RANGE	PIN PACKAGE	FUNCTIONALITY	UVLO, V_{IN} CLAMP	D_{MAX}
MAX17595ATE+	-40°C to +125°C	16 TQFN-EP*	Offline Flyback Controller	20V, Yes	46%
MAX17596ATE+	-40°C to +125°C	16 TQFN-EP*	Low-Voltage DC-DC Flyback Controller	4V, No	46%
MAX17597ATE+	-40°C to +125°C	16 TQFN-EP*	Boost Controller	4V, No	93%

+Denotes a lead(Pb)-free/RoHS-compliant package.
**Exposed pad.*

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
16 TQFN	T1633+4	21-0136	90-0032

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/12	Initial release	—

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